Section 13 Watchdog Timer

13.1 Overview

The H8/532 has an on-chip watchdog timer (WDT) module. This module can monitor system operation by requesting a nonmaskable interrupt if a system crash allows the timer count to overflow.

When this watchdog function is not needed, the WDT module can be used as an interval timer. In the interval timer mode, an IRQ_0 interrupt is requested at each counter overflow.

The WDT module is also used in recovering from the software standby mode.

13.1.1 Features

The basic features of the watchdog timer module are summarized as follows:

- Selection of eight clock sources
- Selection of two modes: watchdog timer mode and interval timer mode
- Counter overflow generates an interrupt request
  NMI request in the watchdog timer mode; IRQ_0 request in the interval timer mode.

13.1.2 Block Diagram

Figure 13-1 is a block diagram of the watchdog timer.

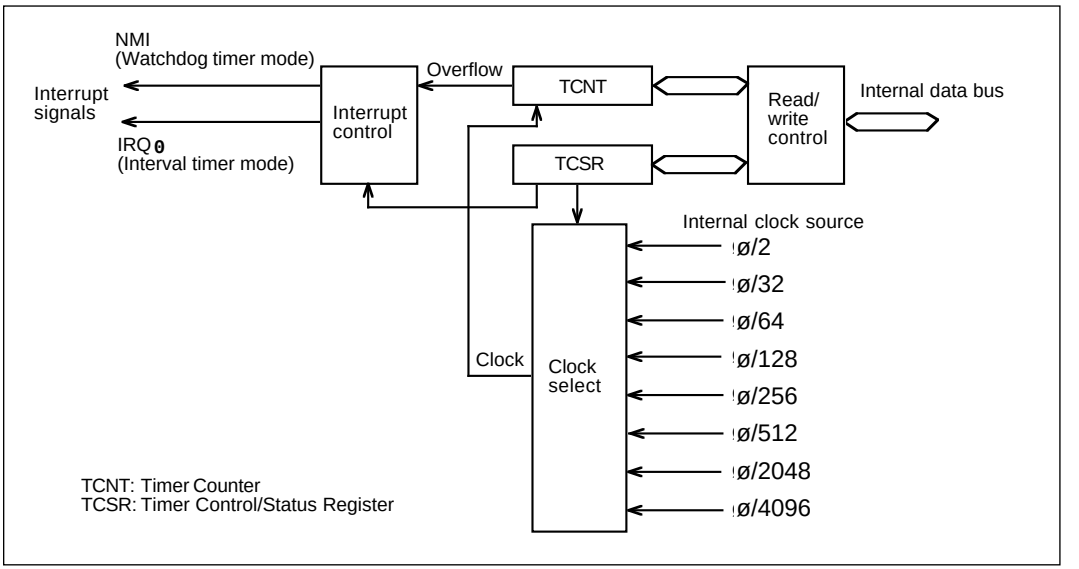

Figure 13-1 Block Diagram of Timer Counter

13.1.3 Register Configuration

Table 13-1 lists information on the watchdog timer registers.

Table 13-1 Register Configuration

			Initial	Addresses	
Name	**Abbreviation**	**R/W**	**Value**	**Write**	**Read**
Timer control/status register	TCSR	R/(W)*	H'18	H'FFED	H'FFEC
Timer counter	TCNT	R/W	H'00	H'FFED	H'FFED

* Software can write a 0 to clear the status flag bits, but cannot write 1.

13.2 Register Descriptions

13.2.1 Timer Counter TCNT—H'FFED

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The watchdog timer counter (TCNT) is a readable/writable* 8-bit up-counter. When the timer enable bit (TME) in the timer control/status register (TCSR) is set to 1, the timer counter starts counting pulses of an internal clock source selected by clock select bits 2 to 0 (CKS2 to CKS0) in the TCSR. When the count overflows (changes from H'FF to H'00), an overflow flag (OVF) in the TCSR is set to 1.

The watchdog timer counter is initialized to H'00 at a reset and when the TME bit is cleared to 0.

* TCNT is write-protected by a password. See section 13.2.3, “Notes on Register Access” for details.

13.2.2 Timer Control/Status Register (TCSR)—H'FFEC (Read), H'FFED (Write)

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{\text{IT}}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)*1	R/W	R/W	—	—	R/W	R/W	R/W

The watchdog timer control/status register (TCSR) is an 8-bit readable/writable*2 register that selects the timer mode and clock source and performs other functions.

Bits 7 to 5 are initialized to 0 at a reset and in the standby modes. Bits 2 to 0 are initialized to 0 at a reset, but retain their values in the standby modes.

*1 Software can write a 0 in bit 7 to clear the flag, but cannot set this bit to 1.
*2 The TCSR is write-protected by a password. See section 13.2.3, “Notes on Register Access” for details.

Bit 7—Overflow Flag (OVF): This bit indicates that the watchdog timer count has overflowed.

Bit 7 OVF	Description	
0	This bit is cleared to from 1 to 0 when the CPU reads the OVF bit, then writes a 0 in this bit.	(Initial value)
1	This bit is set to 1 when TCNT changes from H'FF to H'00.	

Bit 6—Timer Mode Select (WT/$\overline{IT}$): This bit selects whether to operate in the watchdog timer mode or interval timer mode.

Bit 6 WT/$\overline{IT}$	Description	
0	Interval timer mode (IRQ_0 request)	(Initial value)
1	Watchdog timer mode (NMI request)	

Bit 5—Timer Enable (TME): This bit enables or disables the timer.

Bit 5 TME	Description	
0	TCNT is initialized to H'00 and stopped.	(Initial value)
1	TCNT runs. An interrupt is requested when the count overflows.	

Bits 4 and 3—Reserved: These bits cannot be modified and are always read as 1.

Bits 2, 1, and 0—Clock Select (CKS2, CKS1, and CKS0): These bits select one of eight clock sources obtained by dividing the system clock (ø).

The overflow interval listed in the table below is the time from when the watchdog timer counter begins counting from H'00 until an overflow occurs.

In the interval timer mode, IRQ_0 interrupts are requested at this interval.

Bit 2	Bit 1	Bit 0	Description	
CKS2	CKS1	CKS0	Clock Source	Overflow Interval (ø = 10MHz)
0	0	0	ø/2	51.2µs (Initial value)
0	0	1	ø/32	819.2µs
0	1	0	ø/64	1.6ms
0	1	1	ø/128	3.3ms
1	0	0	ø/256	6.6ms
1	0	1	ø/512	13.1ms
1	1	0	ø/2048	52.4ms
1	1	1	ø/4096	104.9ms

13.2.3 Notes on Register Access

The watchdog timer's TCNT and TCSR registers differ from other registers in being more difficult to write. The procedures for writing and reading these registers are given below.

1. **Writing to TCNT and TCSR:** These registers must be written by word access. Programs cannot write to them by byte access. The word must contain the write data and a password.

   The watchdog timer's TCNT and TCSR registers both have the same write address. The write data must be contained in the lower byte of the word written at this address. The upper byte must contain H'5A (password for TCNT) or H'A5 (password for TCSR). See figure 13-2.

   The result of the access depicted in figure 13-2 is to transfer the write data from the lower byte to the TCNT or TCSR.

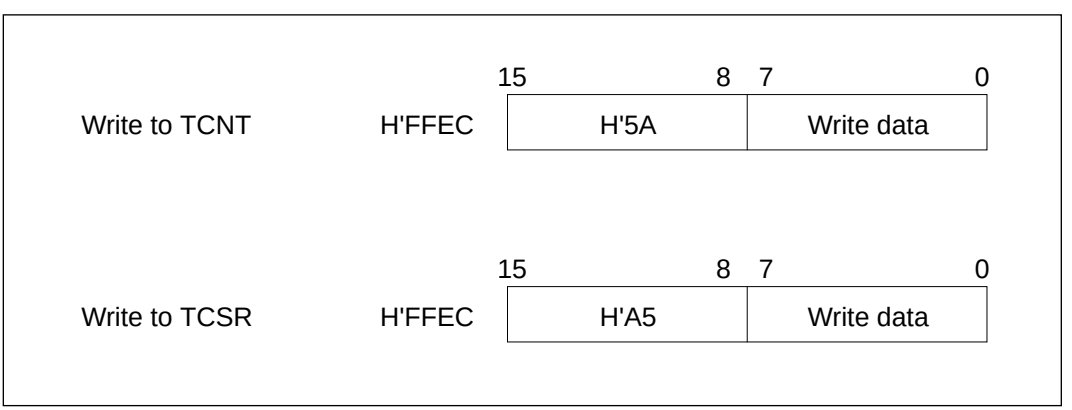

Figure 13-2 Writing to TCNT and TCSR

Coding Examples:

To clear TCNT to 00: `MOV.W #H'5A00, @H'FFEC`

To write H'4F in TCSR: `MOV.W #H'A54F, @H'FFEC`

2. **Reading TCNT and TCSR:** The read addresses are H'FFEC for TCSR and H'FFED for TCNT, as indicated in table 13-2.

   These two registers are read like other registers. Byte access instructions can be used.

Table 13-2 Read Addresses of TCNT and TCSR

Read Address	Register
H'FFEC	TCSR
H'FFED	TCNT

13.3 Operation

13.3.1 Watchdog Timer Mode

The watchdog timer function begins operating when software sets the WT/$\overline{\text{IT}}$ and TME bits to 1 in the TCSR. Thereafter, software should periodically rewrite the contents of the timer counter (normally by writing H'00) to prevent the count from overflowing. If a program crash allows the timer count to overflow, the watchdog timer requests a nonmaskable interrupt (NMI) as shown in figure 13-3.

NMI requests from the watchdog timer have the same vector as NMI requests from the NMI pin, so the NMI interrupt-handling routine must check the OVF bit in the TCSR to determine the source of the interrupt.

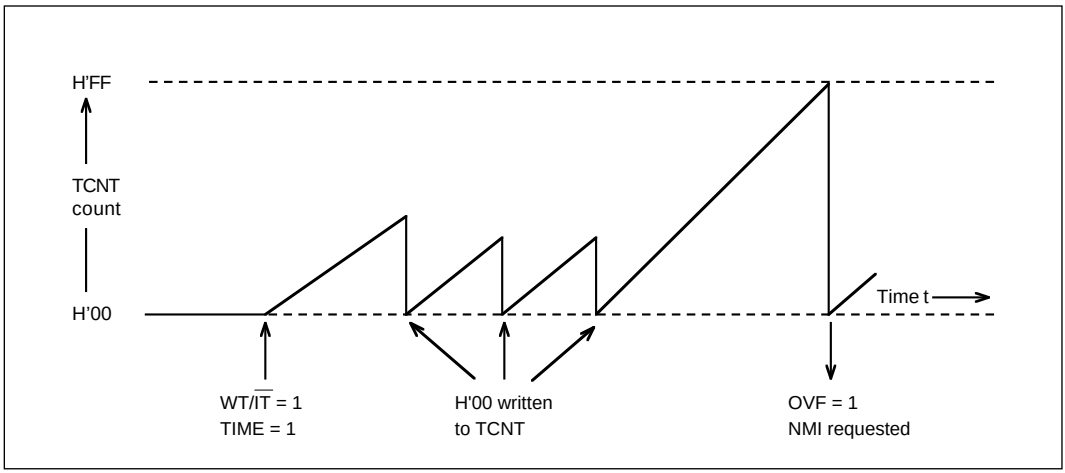

Figure 13-3 Operation in Watchdog Timer Mode

13.3.2 Interval Timer Mode

Interval timer operation begins when the WT/$\overline{IT}$ bit is cleared to 0 and the TME bit is set to 1.

In the interval timer mode, an IRQ0 request is generated each time the timer count overflows. This function can be used to generate IRQ0 requests at regular intervals. See figure 13-4.

IRQ0 requests from the watchdog timer module have the same vector as IRQ0 requests from the $\overline{IRQ0}$ pin, so the IRQ0 interrupt-handling routine must check the OVF bit in the TCSR to determine the source of the interrupt.

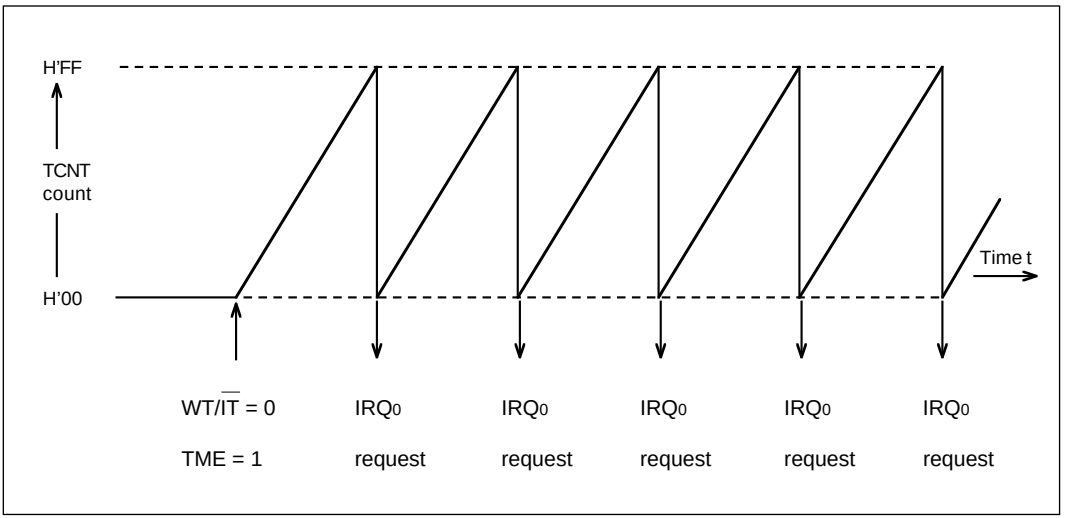

Figure 13-4 Operation in Interval Timer Mode

13.3.3 Operation in Software Standby Mode

The watchdog timer has a special function in the software standby mode. Specific watchdog timer settings are required when the software standby mode is used.

1. **Before Transition to the Software Standby Mode:** The TME bit must be cleared to 0 to stop the watchdog timer counter before a transition to the software standby mode. The chip cannot enter the software standby mode while the TME bit is set to 1. Before entering the software standby mode, software should also set the clock select bits (CKS2 to CKS0) to a value that makes the timer overflow interval equal to or greater than the settling time of the clock oscillator.

2. **Recovery from the Software Standby Mode:** Recovery from the software standby mode can be triggered by an NMI request. In this case the recovery proceeds as follows:

   When an NMI request signal is received, the clock oscillator starts running and the watchdog timer starts counting at the rate selected by the clock select bits before the software standby mode was entered. When the count overflows (H'FF → H'00), the ø clock is presumed to be stable and usable, clock signals are supplied to all modules on the chip, and the NMI interrupt-handling routine starts executing. This timer overflow does not set the OVF flag, and the TME bit remains cleared to 0.

13.3.4 Setting of Overflow Flag

The OVF bit is set to 1 when the timer count overflows. Simultaneously, the WDT module requests an NMI or IRQ0 interrupt. The timing is shown in figure 13-5.

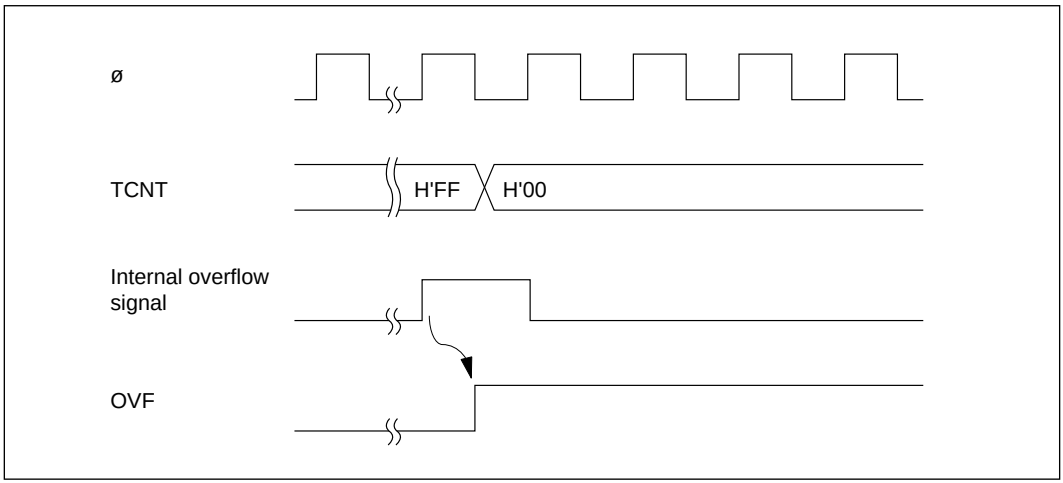

Figure 13-5 Setting of OVF Bit

13.4 Application Notes

1. **Contention between TCNT Write and Increment:** If a timer counter clock pulse is generated during the T3 state of a write cycle to the timer counter, the write takes priority and the timer counter is not incremented. See figure 13-6.

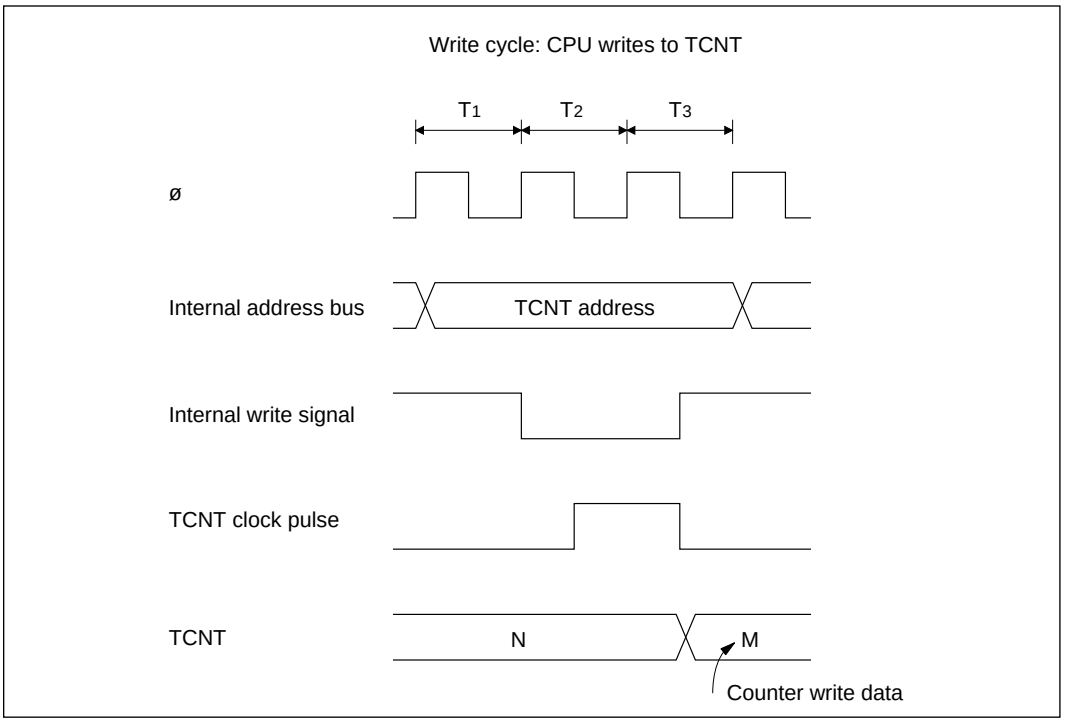

Figure 13-6 TCNT Write-Increment Contention

2. **Changing the Clock Select Bits (CKS2 to CKS0):** Software should stop the watchdog timer (by clearing the TME bit to 0) before changing the value of the clock select bits. If the clock select bits are modified while the watchdog timer is running, the timer count may be incremented incorrectly.