Appendix B Register Field

B.1 Register Addresses and Bit Names

Addr. (last byte)	Register Name	Bit Names								
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Module**
H'80	P1DDR	$P1_7$DDR	$P1_6$DDR	$P1_5$DDR	$P1_4$DDR	$P1_3$DDR	$P1_2$DDR	$P1_1$DDR	$P1_0$DDR	Port 1
H'81	P2DDR	—	—	—	$P2_4$DDR	$P2_3$DDR	$P2_2$DDR	$P2_1$DDR	$P2_0$DDR	Port 2
H'82	P1DR	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$	Port 1
H'83	P1DR	—	—	—	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$	Port 2
H'84	P3DDR	$P3_7$DDR	$P3_6$DDR	$P3_5$DDR	$P3_4$DDR	$P3_3$DDR	$P3_2$DDR	$P3_1$DDR	$P3_0$DDR	Port 3
H'85	P4DDR	$P4_7$DDR	$P4_6$DDR	$P4_5$DDR	$P4_4$DDR	$P4_3$DDR	$P4_2$DDR	$P4_1$DDR	$P4_0$DDR	Port 4
H'86	P3DR	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$	Port 3
H'87	P4DR	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$	Port 4
H'88	P5DDR	$P5_7$DDR	$P5_6$DDR	$P5_5$DDR	$P5_4$DDR	$P5_3$DDR	$P5_2$DDR	$P5_1$DDR	$P5_0$DDR	Port 5
H'89	P6DDR	—	—	—	—	$P6_3$DDR	$P6_2$DDR	$P6_1$DDR	$P6_0$DDR	Port 6
H'8A	P5DR	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$	Port 5
H'8B	P6DR	—	—	—	—	$P6_3$	$P6_2$	$P6_1$	$P6_0$	Port 6
H'8C	P7DDR	$P7_7$DDR	$P7_6$DDR	$P7_5$DDR	$P7_4$DDR	$P7_3$DDR	$P7_2$DDR	$P7_1$DDR	$P7_0$DDR	Port 7
H'8D	—	—	—	—	—	—	—	—	—	—
H'8E	P7DR	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$	Port 7
H'8F	P8DR	$P8_7$	$P8_6$	$P8_5$	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$	Port 8
H'90	TCR	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0	FRT 1
H'91	TCSR	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA	
H'92	FRC (H)									
H'93	FRC (L)									
H'94	OCRA (H)									
H'95	OCRA (L)									
H'96	OCRB (H)									
H'97	OCRB (L)									
H'98	ICR (H)									
H'99	ICR (L)									
H'9A	—	—	—	—	—	—	—	—	—	
H'9B	—	—	—	—	—	—	—	—	—	
H'9C	—	—	—	—	—	—	—	—	—	
H'9D	—	—	—	—	—	—	—	—	—	
H'9E	—	—	—	—	—	—	—	—	—	
H'9F	—	—	—	—	—	—	—	—	—	

Note: (Continued on next page)

FRT1: Free-Running Timer channel 1

(Continued from preceding page)

Addr. (last byte)	Register Name	Bit Names								
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Module**
H'A0	TCR	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0	
H'A1	TCSR	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA	
H'A2	FRC (H)									
H'A3	FRC (L)									
H'A4	OCRA (H)									
H'A5	OCRA (L)									
H'A6	OCRB (H)									
H'A7	OCRB (L)									
H'A8	ICR (H)									FRT2
H'A9	ICR (L)									
H'AA	—	—	—	—	—	—	—	—	—	
H'AB	—	—	—	—	—	—	—	—	—	
H'AC	—	—	—	—	—	—	—	—	—	
H'AD	—	—	—	—	—	—	—	—	—	
H'AE	—	—	—	—	—	—	—	—	—	
H'AF	—	—	—	—	—	—	—	—	—	
H'B0	TCR	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0	
H'B1	TCSR	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA	
H'B2	FRC (H)									
H'B3	FRC (L)									
H'B4	OCRA (H)									
H'B5	OCRA (L)									
H'B6	OCRB (H)									
H'B7	OCRB (L)									
H'B8	ICR (H)									FRT 3
H'B9	ICR (L)									
H'BA	—	—	—	—	—	—	—	—	—	
H'BB	—	—	—	—	—	—	—	—	—	
H'BC	—	—	—	—	—	—	—	—	—	
H'BD	—	—	—	—	—	—	—	—	—	
H'BE	—	—	—	—	—	—	—	—	—	
H'BF	—	—	—	—	—	—	—	—	—	

Notes:

(Continued on next page)

FRT2: Free-Running Timer channel 2

FRT3: Free-Running Timer channel 3

(Continued from preceding page)

Addr. (last byte)	Register Name	Bit Names								
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
H'C0	TCR	OE	OS	—	—	—	CKS2	CKS1	CKS0	PWM1
H'C1	DTR									
H'C2	TCNT									
H'C3	—	—	—	—	—	—	—	—	—	
H'C4	TCR	OE	OS	—	—	—	CKS2	CKS1	CKS0	PWM2
H'C5	DTR									
H'C6	TCNT									
H'C7	—	—	—	—	—	—	—	—	—	
H'C8	TCR	OE	OS	—	—	—	CKS2	CKS1	CKS0	PWM3
H'C9	DTR									
H'CA	TCNT									
H'CB	—	—	—	—	—	—	—	—	—	
H'CC	—	—	—	—	—	—	—	—	—	—
H'CD	—	—	—	—	—	—	—	—	—	
H'CE	—	—	—	—	—	—	—	—	—	
H'CF	—	—	—	—	—	—	—	—	—	
H'D0	TCR	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR
H'D1	TCSR	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	
H'D2	TCORA									
H'D3	TCORB									
H'D4	TCNT									
H'D5	—	—	—	—	—	—	—	—	—	
H'D6	—	—	—	—	—	—	—	—	—	
H'D7	—	—	—	—	—	—	—	—	—	
H'D8	SMR	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	—	CKS1	CKS0	SCI
H'D9	BRR									
H'DA	SCR	TIE	RIE	TE	RE	—	—	CKE1	CKE0	
H'DB	TDR									
H'DC	SSR	TDRE	RDRF	ORER	FER	PER	—	—	—	
H'DD	RDR									
H'DE	—	—	—	—	—	—	—	—	—	
H'DF	—	—	—	—	—	—	—	—	—	

Notes:

(Continued on next page)

PWM1: Pulse-Width Modulation timer channel 1
PWM2: Pulse-Width Modulation timer channel 2
PWM3: Pulse-Width Modulation timer channel 3
TMR: 8-Bit Timer
SCI: Serial Communication Interface

(Continued from preceding page)

Addr. (last byte)	Register Name	Bit Names								
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Module**
H'E0	ADDRA (H)	AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	A/D
H'E1	ADDRA (L)	AD_1	AD_0	—	—	—	—	—	—	
H'E2	ADDRB (H)	AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	
H'E3	ADDRB (L)	AD_1	AD_0	—	—	—	—	—	—	
H'E4	ADDRC (H)	AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	
H'E5	ADDRC (L)	AD_1	AD_0	—	—	—	—	—	—	
H'E6	ADDRD (H)	AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2	
H'E7	ADDRD (L)	AD_1	AD_0	—	—	—	—	—	—	
H'E8	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
H'E9	—	—	—	—	—	—	—	—	—	
H'EA	—	—	—	—	—	—	—	—	—	
H'EB	—	—	—	—	—	—	—	—	—	
H'EC	TCSR*	OVF	$WT/\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0	WDT
H'ED	TCNT*	—	—	—	—	—	—	—	—	
H'EE	—	—	—	—	—	—	—	—	—	—
H'EF	—	—	—	—	—	—	—	—	—	

Notes: (Continued on next page)

A/D: Analog-to-Digital converter

WDT: Watchdog Timer

* Read addresses are shown. Write addresses of both TCSR and TCNT are H'FFED. See section 13.2.3, “Notes on Register Access” for details.

(Continued from preceding page)

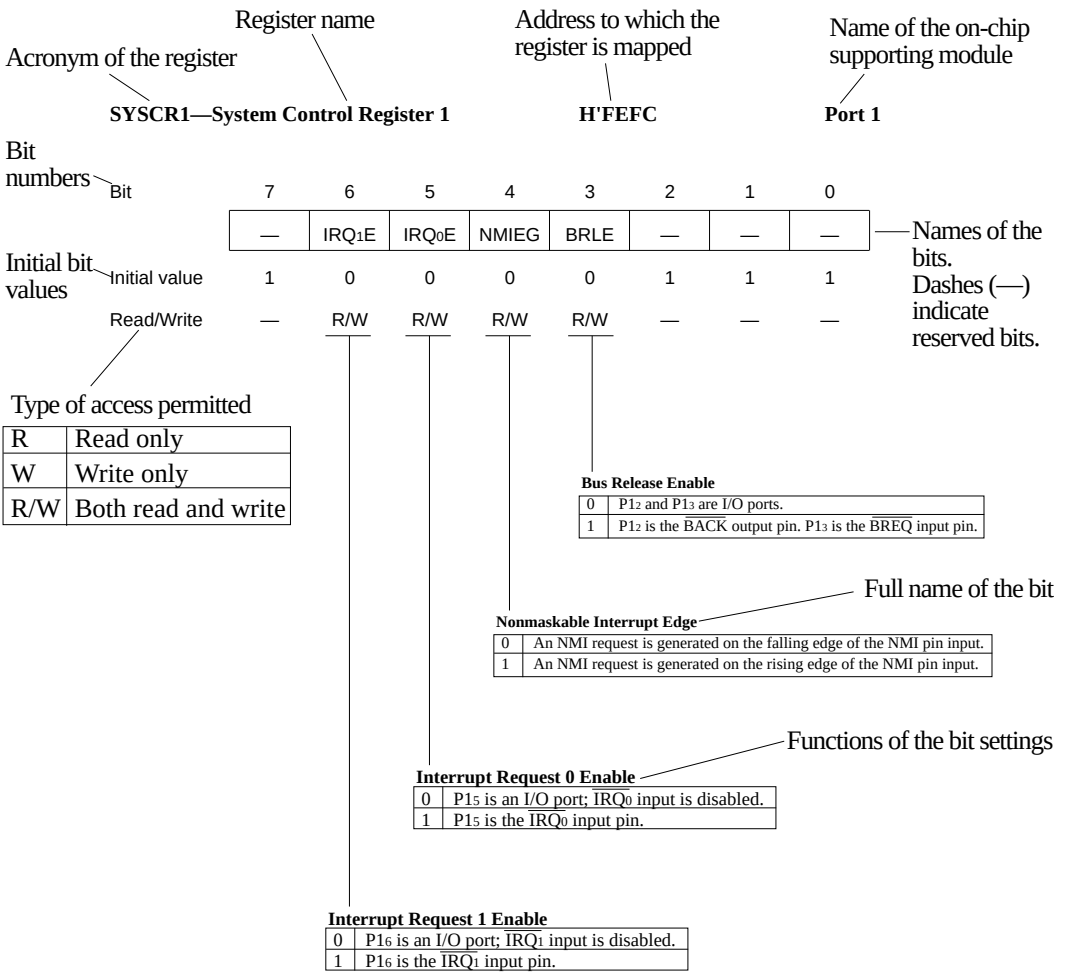
Addr. (last byte)	Register Name	Bit Names								
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Module**
H'F0	IPRA	—	IRQ$_0$			—	IRQ$_1$			INTC
H'F1	IPRB	—	FRT$_1$			—	FRT$_2$			
H'F2	IPRC	—	FRT$_3$			—	8 Bit Timer			
H'F3	IPRD	—	SCI			—	A/D			
H'F4	DTEA	—	—	—	IRQ$_0$	—	—	—	IRQ$_1$	
H'F5	DTEB	—	OCIB1	OCIA1	ICI1	—	OCIB2	OCIA2	ICI2	
H'F6	DTEC	—	OCIB3	OCIA3	ICI3	—	—	CMIB	CMIA	
H'F7	DTED	—	TXI	RXI	—	—	—	—	ADI	
H'F8	WCR	—	—	—	—	WMS1	WMS0	WC1	WC0	WSC
H'F9	RAMCR	RAME	—	—	—	—	—	—	—	RAM
H'FA	MDCR	—	—	—	—	—	MDS2	MDS1	MDS0	
H'FB	SBYCR	SSBY	—	—	—	—	—	—	—	
H'FC	P1CR	—	IRQ$_1$E	IRQ$_0$E	NMIEG	BRLE	—	—	—	Port 1
H'FD	—	—	—	—	—	—	—	—	—	
H'FE	P9DDR	P9$_7$DDR	P9$_6$DDR	P9$_5$DDR	P9$_4$DDR	P9$_3$DDR	P9$_2$DDR	P9$_1$DDR	P9$_0$DDR	Port 9
H'FF	P9DR	P9$_7$	P9$_6$	P9$_5$	P9$_4$	P9$_3$	P9$_2$	P9$_1$	P9$_0$	

Notes:

INTC: Interrupt Controller

WSC: Wait State Controller

B.2 Register Descriptions



P1DDR—Port 1 Data Direction Register **H'FF80** **Port 1**

Bit	7	6	5	4	3	2	1	0
	$P1_7DDR$	$P1_6DDR$	$P1_5DDR$	$P1_4DDR$	$P1_3DDR$	$P1_2DDR$	$P1_1DDR$	$P1_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 1 Input/Output Selection

0	Input port
1	Output port

P1DR—Port 1 Data Register **H'FF82** **Port 1**

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

P1CR—Port 1 Control Register **H'FFFC** **Port 1**

Bit	7	6	5	4	3	2	1	0
	—	IRQ1E	IRQ0E	NMIEG	BRLE	—	—	—
Initial value	1	0	0	0	0	1	1	1
Read/Write	—	R/W	R/W	R/W	R/W	—	—	—

Bus Release Enable

0	P12 and P13 are I/O ports.
1	P12 is the output pin and P13 is the input pin.

Nonmaskable Interrupt Edge

0	An NMI request is generated on the falling edge of the NMI pin input.
1	An NMI request is generated on the rising edge of the NMI pin input.

Interrupt Request 0 Enable

0	P15 is an I/O port; input is disabled.
1	P15 is the input pin.

Interrupt Request 1 Enable

0	P16 is an I/O port; input is disabled.
1	P16 is the input pin.

P2DDR—Port 2 Data Direction Register **H'FF81** **Port 2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	W	W	W	W	W

Port 2 Input/Output Selection

0	Input port
1	Output port

P2DR—Port 2 Data Register **H'FF83** **Port 2**

Bit	7	6	5	4	3	2	1	0
	—	—	—	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

P3DDR—Port 3 Data Direction Register **H'FF84** **Port 3**

Bit	7	6	5	4	3	2	1	0
	$P3_7$DDR	$P3_6$DDR	$P3_5$DDR	$P3_4$DDR	$P3_3$DDR	$P3_2$DDR	$P3_1$DDR	$P3_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 3 Input/Output Selection

0	Input port
1	Output port

P3DR—Port 3 Data Register **H'FF86** **Port 3**

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P4DDR—Port 4 Data Direction Register **H'FF85** **Port 4**

Bit	7	6	5	4	3	2	1	0
	$P4_7$DDR	$P4_6$DDR	$P4_5$DDR	$P4_4$DDR	$P4_3$DDR	$P4_2$DDR	$P4_1$DDR	$P4_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 4 Input/Output Selection

0	Input port
1	Output port

P4DR—Port 4 Data Register **H'FF87** **Port 4**

Bit	7	6	5	4	3	2	1	0
	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P5DDR—Port 5 Data Direction Register **H'FF88** **Port 5**

Bit	7	6	5	4	3	2	1	0
	$P5_7$DDR	$P5_6$DDR	$P5_5$DDR	$P5_4$DDR	$P5_3$DDR	$P5_2$DDR	$P5_1$DDR	$P5_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 5 Input/Output Selection

0	Input port
1	Output port

P5DR—Port 5 Data Register **H'FF8A** **Port 5**

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P6DDR—Port 6 Data Direction Register **H'FF89** **Port 6**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P6_3$DDR	$P6_2$DDR	$P6_1$DDR	$P6_0$DDR
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

Port 6 Input/Output Selection

0	Input port
1	Output port

P6DR—Port 6 Data Register **H'FF8B** **Port 6**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

P7DDR—Port 7 Data Direction Register **H'FF8C** **Port 7**

Bit	7	6	5	4	3	2	1	0
	$P7_7$DDR	$P7_6$DDR	$P7_5$DDR	$P7_4$DDR	$P7_3$DDR	$P7_2$DDR	$P7_1$DDR	$P7_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 7 Input/Output Selection

0	Input port
1	Output port

P7DR—Port 7 Data Register **H'FF8E** **Port 7**

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P8DR—Port 8 Data Register **H'FF8F** **Port 8**

Bit	7	6	5	4	3	2	1	0
	$P8_7$	$P8_6$	$P8_5$	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$
Read/Write	R	R	R	R	R	R	R	R

P9DDR—Port 9 Data Direction Register **H'FFFE** **Port 9**

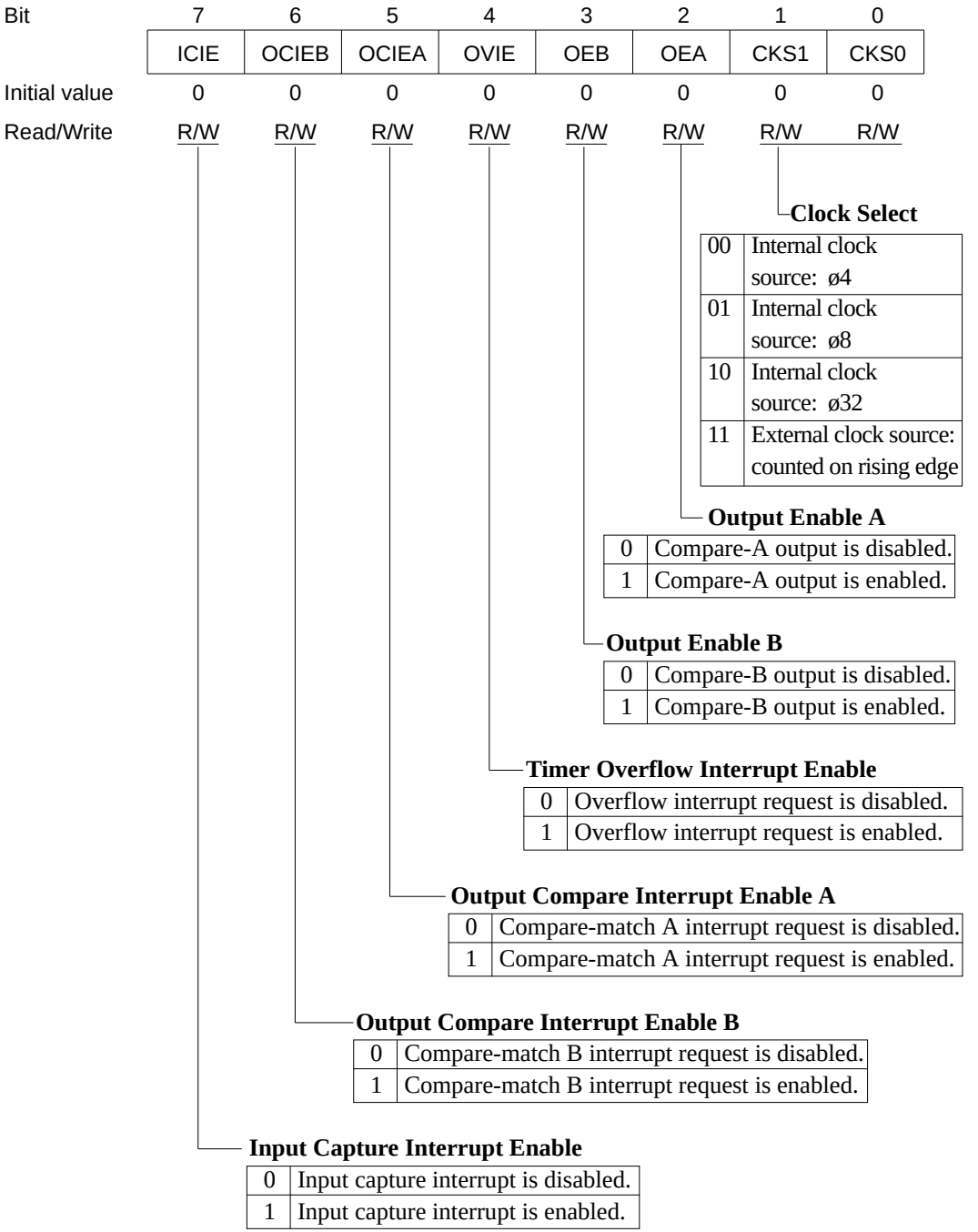
Bit	7	6	5	4	3	2	1	0
	$P9_7DDR$	$P9_6DDR$	$P9_5DDR$	$P9_4DDR$	$P9_3DDR$	$P9_2DDR$	$P9_1DDR$	$P9_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

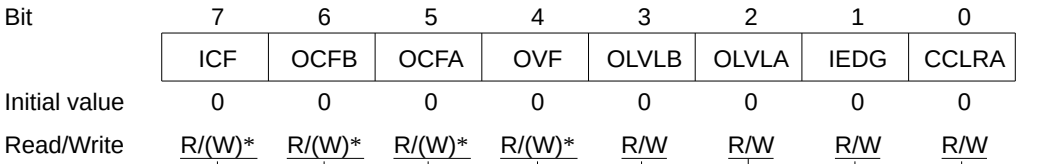
Port 9 Input/Output Selection

0	Input port
1	Output port

P9DR—Port 9 Data Register **H'FFFF** **Port 9**

Bit	7	6	5	4	3	2	1	0
	$P9_7$	$P9_6$	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W


Bit
7 6 5 4 3 2 1 0
ICIE OCIEB OCIEA OVIE OEB OEA CKS1 CKS0
Initial value
0 0 0 0 0 0 0 0
Read/Write
R/W R/W R/W R/W R/W R/W R/W R/W
Clock Select
00 Internal clock source: ø4
01 Internal clock source: ø8
10 Internal clock source: ø32
11 External clock source: counted on rising edge
Output Enable A
0 Compare-A output is disabled.
1 Compare-A output is enabled.
Output Enable B
0 Compare-B output is disabled.
1 Compare-B output is enabled.
Timer Overflow Interrupt Enable
0 Overflow interrupt request is disabled.
1 Overflow interrupt request is enabled.
Output Compare Interrupt Enable A
0 Compare-match A interrupt request is disabled.
1 Compare-match A interrupt request is enabled.
Output Compare Interrupt Enable B
0 Compare-match B interrupt request is disabled.
1 Compare-match B interrupt request is enabled.
Input Capture Interrupt Enable
0 Input capture interrupt is disabled.
1 Input capture interrupt is enabled.



Bit	7	6	5	4	3	2	1	0
	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W

Counter Clear A

0	FRC count is not cleared.
1	FRC count is cleared by compare-match A.

Input Edge Select

0	Count is captured on falling edge of input capture signal (FTI).
1	Count is captured on rising edge of input capture signal.

Output Level A

0	Compare-match A causes 0 output.
1	Compare-match A causes 1 output.

Output Level B

0	Compare-match B causes 0 output.
1	Compare-match B causes 1 output.

Timer Overflow

0	Cleared from 1 to 0 when CPU reads OVF = 1, then writes 0 in OVF.
1	Set to 1 when FRC changes from H'FFFF to H'0000.

Output Compare Flag A

0	Cleared from 1 to 0 when: 1. CPU reads OCFA = 1, then writes 0 in OCFA. 2. OCIA interrupt is served by DTC.
1	Set to 1 when FRC = OCRA.

Output Compare Flag B

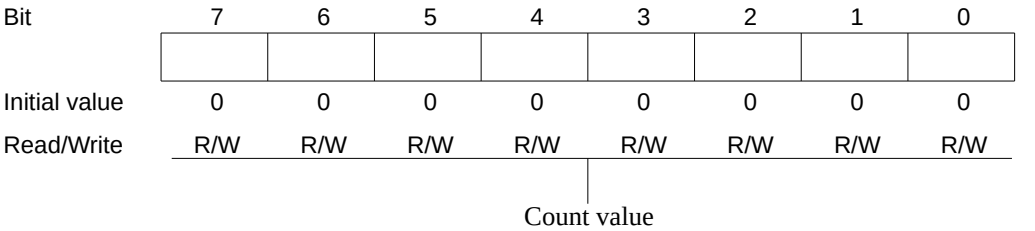
0	Cleared from 1 to 0 when: 1. CPU reads OCFB = 1, then writes 0 in OCFB. 2. OCIB interrupt is served by DTC.
1	Set to 1 when FRC = OCRB.

Input Capture Flag

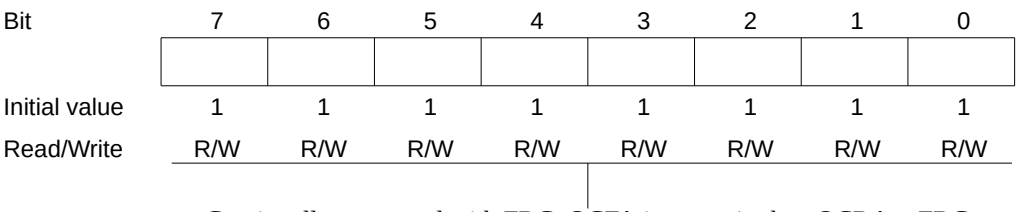
0	Cleared from 1 to 0 when: 1. CPU reads ICF = 1, then writes 0 in ICF. 2. ICI interrupt is served by DTC.
1	Set to 1 when input capture signal is received and FRC count is copied to ICR.

* Only writing of a 0 to clear the flag is enabled.

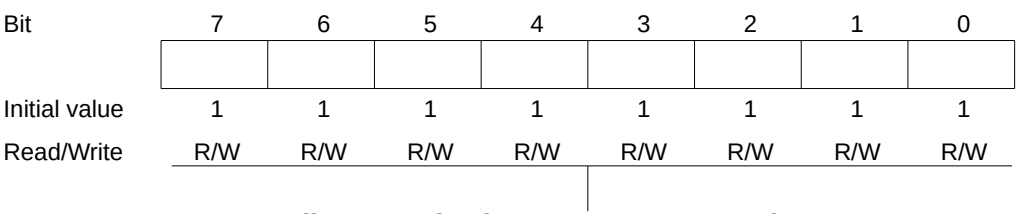
FRC (H and L)—Free-Running Counter H'FF92, H'FF93 FRT 1



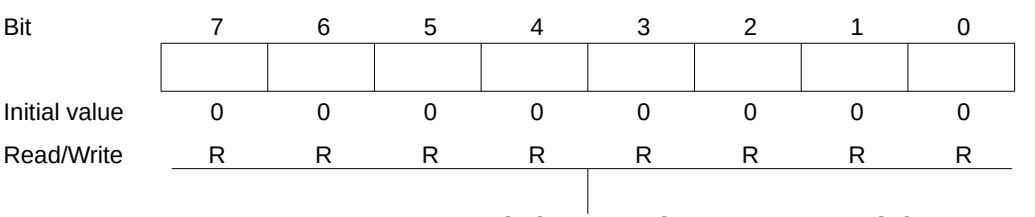
OCRA (H and L)—Output Compare Register A H'FF94, H'FF95 FRT 1



OCRB (H and L)—Output Compare Register B H'FF96, H'FF97 FRT 1



ICR (H and L)—Input Capture Register H'FF98, H'FF99 FRT 1



TCR—Timer Control Register **H'FFA0** **FRT 2**

Bit	7	6	5	4	3	2	1	0
	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

TCSR—Timer Control/Status Register **H'FFA1** **FRT 2**

Bit	7	6	5	4	3	2	1	0
	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

* Only writing of a 0 to clear the flag is enabled.

FRC (H and L)—Free-Running Counter **H'FFA2, H'FFA3** **FRT 2**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

OCRA (H and L)—Output Compare Register A H'FFA4, H'FFA5 FRT 2

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

OCRB (H and L)—Output Compare Register B H'FFA6, H'FFA7 FRT 2

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

ICR (H and L)—Input Capture Register H'FFA8, H'FFA9 FRT 2

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Note: Bit functions are the same as for FRT1.

TCR—Timer Control Register H'FFB0 FRT 3

Bit	7	6	5	4	3	2	1	0
	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

TCSR—Timer Control/Status Register **H'FFB1** **FRT 3**

Bit	7	6	5	4	3	2	1	0
	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

* Only writing of 0 to clear the flag is enabled.

FRC (H and L)—Free-Running Counter **H'FFB2, H'FFB3** **FRT 3**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

OCRA (H and L)—Output Compare Register A **H'FFB4, H'FFB5** **FRT 3**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

OCRB (H and L)—Output Compare Register B H'FFB6, H'FFB7 FRT 3

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for FRT1.

ICR (H and L)—Input Capture Register H'FFB8, H'FFB9 FRT 3

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Note: Bit functions are the same as for FRT1.

TCR—Timer Control Register **H'FFC0** **PWM1**

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

Clock Select (Values When ø = 10MHz)

	Internal Clock Freq.	Reso-lution	PW Period	PW Frequency
000	ø/2	200ns	50µs	20kHz
001	ø/8	800ns	200µs	5kHz
010	ø/32	3.2µs	800µs	1.25kHz
011	ø/128	12.8µs	3.2ms	312.5kHz
100	ø/256	25.6µs	6.4ms	156.3Hz
101	ø/1024	102.4µs	25.6ms	39.1Hz
110	ø/2048	204.8µs	51.2ms	19.5Hz
111	ø/4096	409.6µs	102.4ms	9.8Hz

Output Select

0	Positive logic
1	Negative logic

Output Enable

0	PW output disabled; TCNT cleared to H'00 and stops.
1	PW output enabled; TCNT runs.

DTR—Duty Register **H'FFC1** **PWM1**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Pulse duty factor

TCNT—Timer Counter **H'FFC2** **PWM1**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Count value (runs from H'00 to H'F9, then repeats from H'00)

* Write function is for test purposes only. Writing to this register during normal operation may have unpredictable effects

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TCR—Timer Control Register **H'FFC4** **PWM2**

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

Note: Bit functions are the same as for PWM1.

DTR—Duty Register **H'FFC5** **PWM2**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Bit functions are the same as for PWM1.

TCNT—Timer Counter **H'FFC6** **PWM2**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: Bit functions are the same as for PWM1.

* Write function is for test purposes only. Writing to this register during normal operation may have unpredictable effects

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TCR—Timer Control Register **H'FFC8** **PWM3**

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

Note: Bit functions are the same as for PWM1.

DTR—Duty Register **H'FFC9** **PWM3**

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

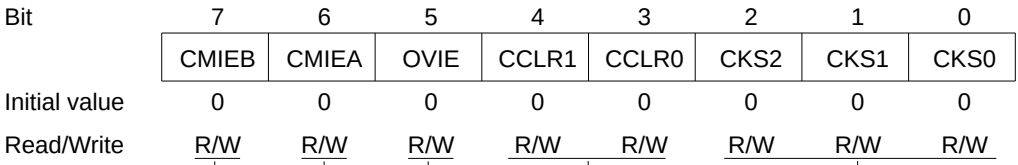
Note: Bit functions are the same as for PWM1.

TCNT—Timer Counter **H'FFCA** **PWM3**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: Bit functions are the same as for PWM1.

* Write function is for test purposes only. Writing to this register during normal operation may have unpredictable effects.



Bit	7	6	5	4	3	2	1	0
	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	0	No clock source; timer stops.
0	0	1	Internal clock source: ø8, counted on falling edge.
0	1	0	Internal clock source: ø64, counted on falling edge.
0	1	1	Internal clock source: ø1024, counted on falling edge.
1	0	0	No clock source; timer stops.
1	0	1	External clock source, counted on rising edge.
1	1	0	External clock source, counted on falling edge.
1	1	1	External clock source, counted on both rising and falling edges.

Counter Clear

0	0	Counter is not cleared.
0	1	Cleared by compare-match A.
1	0	Cleared by compare-match B.
1	1	Cleared on rising edge of external reset input.

Timer Overflow Interrupt Enable

0	Overflow interrupt request is disabled.
1	Overflow interrupt request is enabled.

Compare-Match Interrupt Enable A

0	Compare-match A interrupt request is disabled.
1	Compare-match A interrupt request is enabled.

Compare-Match Interrupt Enable B

0	Compare-match B interrupt request is disabled.
1	Compare-match B interrupt request is enabled.

Bit	7	6	5	4	3	2	1	0
	CMFB	CMFA	OVF	—	OS3*2	OS2*2	OS1*2	OS0*2
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/(W)*1	R/(W)*1	R/(W)*1	—	R/W	R/W	R/W	R/W

Output Select

0	0	No change on compare-match A.
0	1	Output 0 on compare-match A.
1	0	Output 1 on compare-match A.
1	1	Invert (toggle) output on compare-match A.

Output Select

0	0	No change on compare-match B.
0	1	Output 0 on compare-match B.
1	0	Output 1 on compare-match B.
1	1	Invert (toggle) output on compare-match B.

Timer Overflow Flag

0	Cleared from 1 to 0 when CPU reads OVF = 1, then writes 0 in OVF.
1	Set to 1 when TCNT changes from H'FF to H'00.

Compare-Match Flag A

0	Cleared from 1 to 0 when: 1. CPU reads CMFA = 1, then writes 0 in CMFA. 2. CMA interrupt is served by the DTC.
1	Set to 1 when TCNT = TCORA.

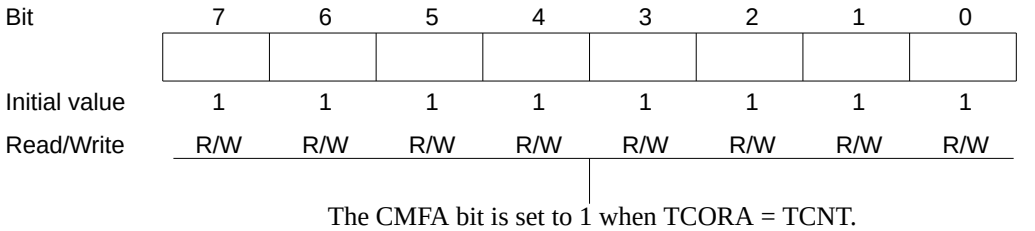
Compare-Match Flag B

0	Cleared from 1 to 0 when: 1. CPU reads CMFB = 1, then writes 0 in CMFB. 2. CMB interrupt is served by the DTC.
1	Set to 1 when TCNT = TCORB.

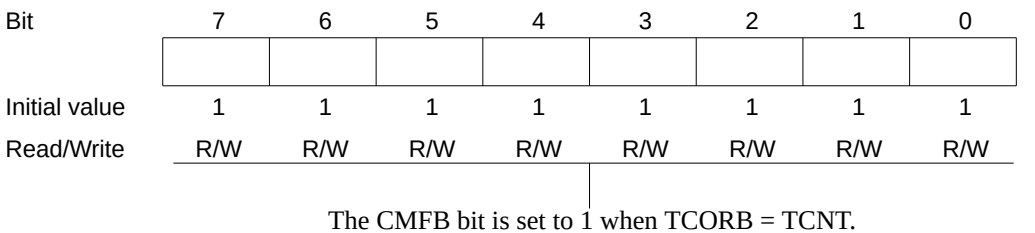
*1 Only writing of 0 to clear the flag is enabled.

*2 When all four bits (OS3 to OS0) are cleared to 0, output is disabled.

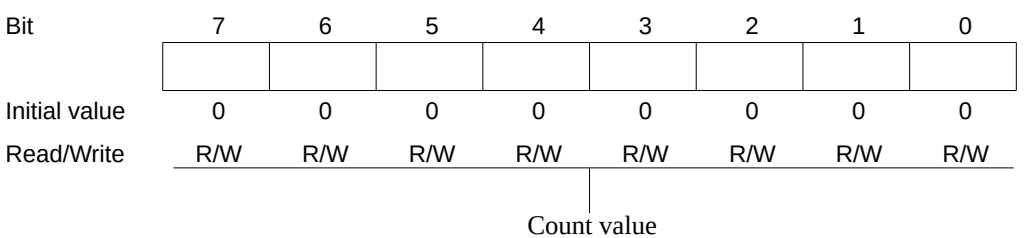
TCORA—Time Constant Register A **H'FFD2** **TMR**

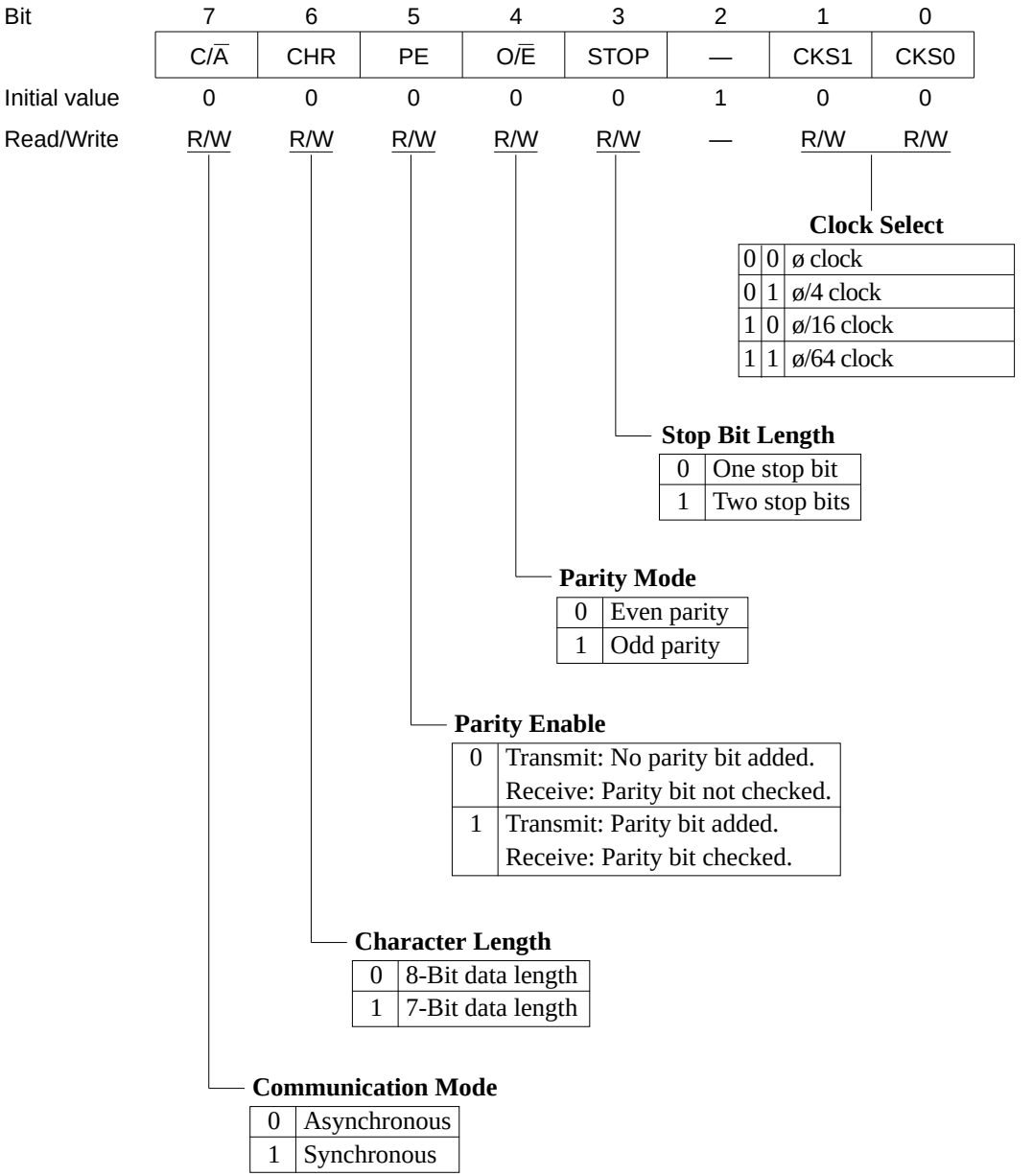


TCORB—Time Constant Register B **H'FFD3** **TMR**

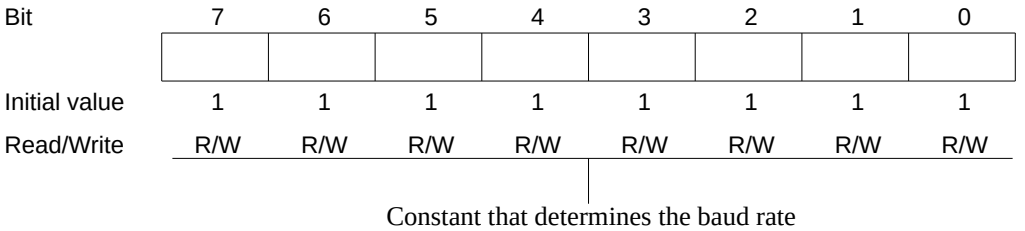


TCNT—Timer Counter **H'FFD4** **TMR**

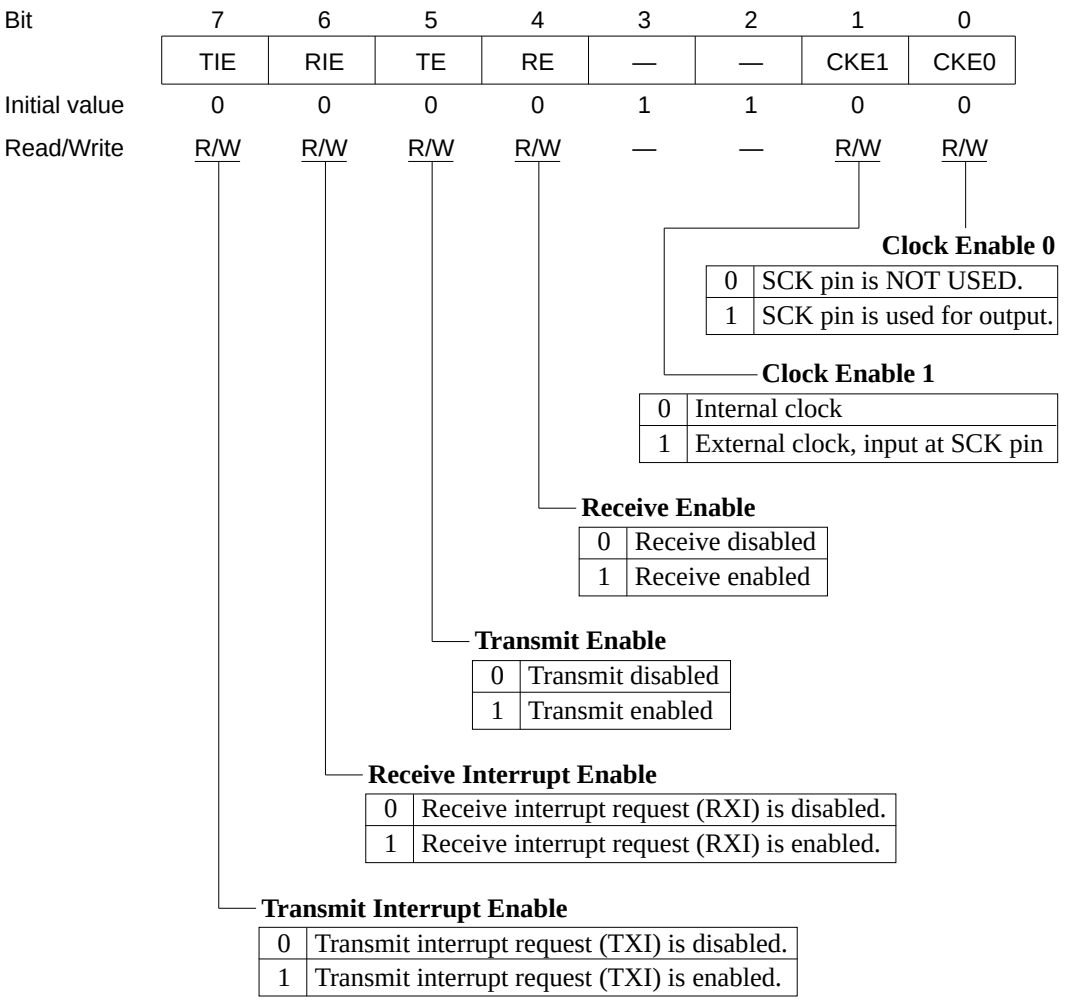



Bit
7
6
5
4
3
2
1
0
C/$\overline{A}$
CHR
PE
O/$\overline{E}$
STOP
—
CKS1
CKS0
Initial value
0
0
0
0
0
1
0
0
Read/Write
R/W
R/W
R/W
R/W
R/W
—
R/W
R/W
Clock Select
0 0 ø clock
0 1 ø/4 clock
1 0 ø/16 clock
1 1 ø/64 clock
Stop Bit Length
0 One stop bit
1 Two stop bits
Parity Mode
0 Even parity
1 Odd parity
Parity Enable
0 Transmit: No parity bit added.
Receive: Parity bit not checked.
1 Transmit: Parity bit added.
Receive: Parity bit checked.
Character Length
0 8-Bit data length
1 7-Bit data length
Communication Mode
0 Asynchronous
1 Synchronous

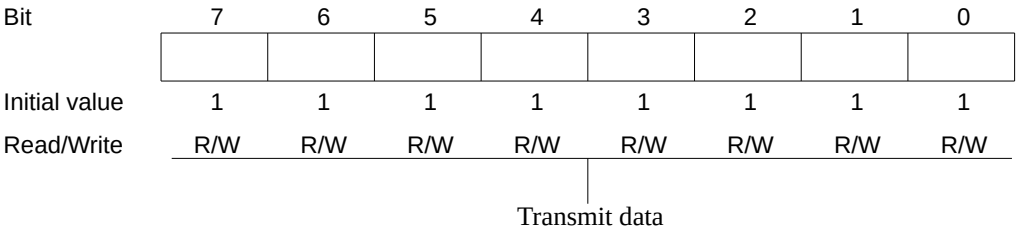
BRR—Bit Rate Register **H'FFD9** **SCI**



SCR—Serial Control Register **H'FFDA** **SCI**



TDR—Transmit Data Register **H'FFDB** **SCI**



Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	ORER	FER	PER	—	—	—
Initial value	1	0	0	0	0	1	1	1
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	—	—	—

Parity Error

0	Cleared from 1 to 0 when: 1. CPU reads PER = 1, then writes 0 in PER. 2. The chip is reset or enters a standby mode.
1	Set to 1 when a parity error occurs (parity of receive data does not match parity selected by bit).

Framing Error

0	Cleared from 1 to 0 when: 1. CPU reads FER = 1, then writes 0 in FER. 2. The chip is reset or enters a standby mode.
1	Set to 1 when a framing error occurs (stop bit is 0).

Overrun Error

0	Cleared from 1 to 0 when: 1. CPU reads ORER = 1, then writes 0 in ORER. 2. The chip is reset or enters a standby mode.
1	Set to 1 when an overrun error occurs (next data is completely received while RDRF bit is set to 1).

Receive Data Register Full

0	Cleared from 1 to 0 when: 1. CPU reads RDRF = 1, then writes 0 in RDRF. 2. RDR is read by the DTC. 3. The chip is reset or enters a standby mode.
1	Set to 1 when one character is received normally and transferred from RSR to RDR.

Transmit Data Register Empty

0	Cleared from 1 to 0 when: 1. CPU reads TDRE = 1, then writes 0 in TDRE. 2. The DTC writes data in TDR.
1	Set to 1 when: 1. The chip is reset or enters a standby mode. 2. Data is transferred from TDR to TSR. 3. CPU reads TDRE = 0, then clears 0 in TE.

* Only writing of 0 to clear the flag is enabled.

RDR—Receive Data Register **H'FFDD** **SCI**

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Receive data

ADDRn (H)—A/D Data Register n (High)
H'FFE0, H'FFE2, H'FFE4, H'FFE6 **(n = A, B, C, D)** **A/D**

Bit	7	6	5	4	3	2	1	0
	AD_9	AD_8	AD_7	AD_6	AD_5	AD_4	AD_3	AD_2
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Upper 8 bits of 10-bit A/D conversion result

ADDRn (L)—A/D Data Register n (Low)
H'FFE1, H'FFE3, H'FFE5, H'FFE7 **(n = A, B, C, D)** **A/D**

Bit	7	6	5	4	3	2	1	0
	AD_1	AD_0	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

Lower 2 bits of 10-bit A/D conversion result

Bit	7	6	5	4	3	2	1	0
	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Channel Select

CH2	CH1	CH0	Single Mode	Scan Mode
0	0	0	AN_0	AN_0
	0	1	AN_1	AN_0, AN_1
	1	0	AN_2	AN_0 to AN_2
	1	1	AN_3	AN_0 to AN_3
1	0	0	AN_4	AN_4
	0	1	AN_5	AN_4, AN_5
	1	0	AN_6	AN_4 to AN_6
	1	1	AN_7	AN_4 to AN_7

Clock Select

0	Conversion time = 274 states
1	Conversion time = 138 states

Scan Mode

0	Single mode
1	Scan mode

A/D Start

0	A/D conversion is halted.
1	1. Single mode: One A/D conversion is performed, then this bit is automatically cleared to 0. 2. Scan mode: A/D conversion starts and continues cyclically on all selected channels until 0 is written in this bit.

A/D Interrupt Enable

0	The A/D interrupt request (ADI) is disabled.
1	The A/D interrupt request (ADI) is enabled.

A/D End Flag

0	Cleared from 1 to 0 when: 1. The chip is reset or enters a standby mode. 2. CPU reads ADF = 1, then writes 0 in ADF. 3. DTC is served by ADI.
1	Set to 1 at the following times: 1. Single mode: at the completion of A/D conversion. 2. Scan mode: when all selected channels have been converted.

* Only writing of 0 to clear the flag is enabled.

TCSR—Timer Status/Control Register **H'FFEC[*1], H'FFED[*2]** **WDT**

Bit	7	6	5	4	3	2	1	0
	OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/(W)[*3]	R/W	R/W	—	—	R/W	R/W	R/W

Clock Select

0	0	0	ø/2	(51.2µs)[*4]
0	0	1	ø/32	(819.2µs)
0	1	0	ø/64	(1.6ms)
0	1	1	ø/128	(3.3ms)
1	0	0	ø/256	(6.6ms)
1	0	1	ø/512	(13.1ms)
1	1	0	ø/2048	(52.4ms)
1	1	1	ø/4096	(104.9ms)

Timer Enable

0	Timer is disabled. • TCNT is initialized to H'00 and stopped.
1	Timer is enabled. • TCNT starts incrementing. • CPU interrupt request is enabled.

Timer Mode Select

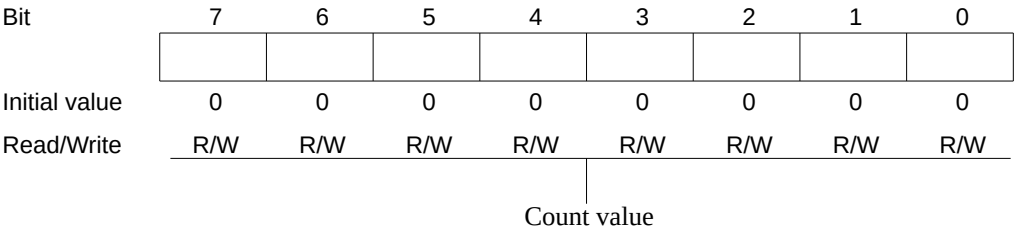
0	Interval timer mode (IRQ0 interrupt request)
1	Watchdog timer mode (NMI interrupt request)

Overflow Flag

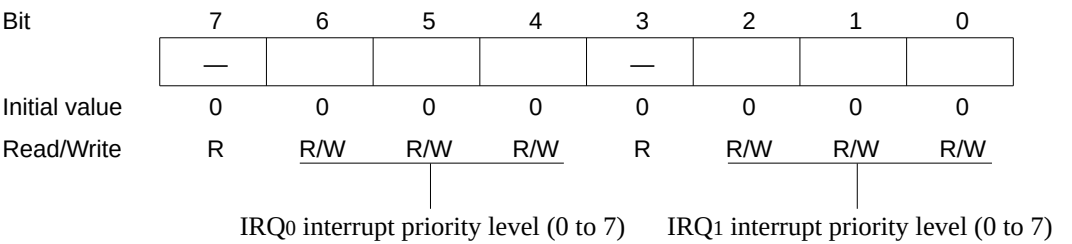
0	Cleared from 1 to 0 when CPU reads OVF = 1, then wtites 0 in OVF.
1	Set to 1 when TCNT changes from H'FF to H'00.

*1 Read address
*2 Write address
*3 Only writing of 0 to clear the flag is enabled.
*4 Times in parentheses are the times for TCNT to increment from H'00 to H'FF and change to H'00 again when ø = 10MHz.

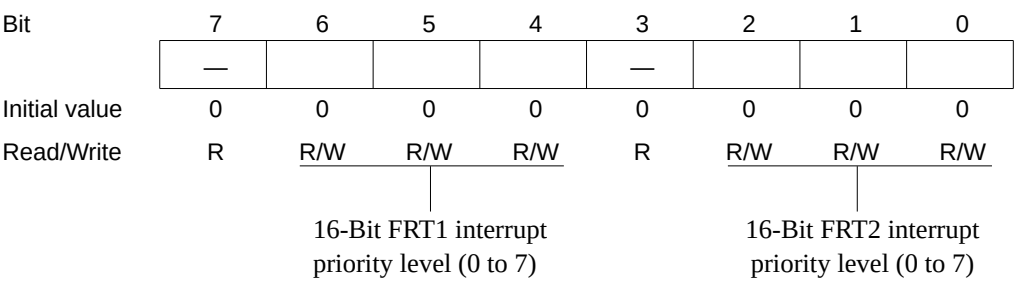
TCNT—Timer Counter **H'FFED** **WDT**



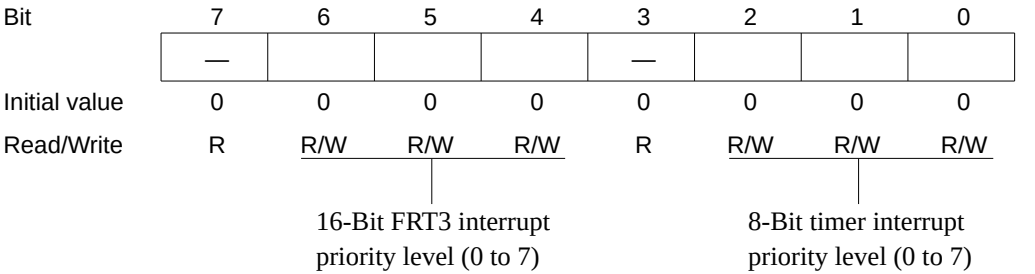
IPRA—Interrupt Priority Register A **H'FFF0** **INTC**



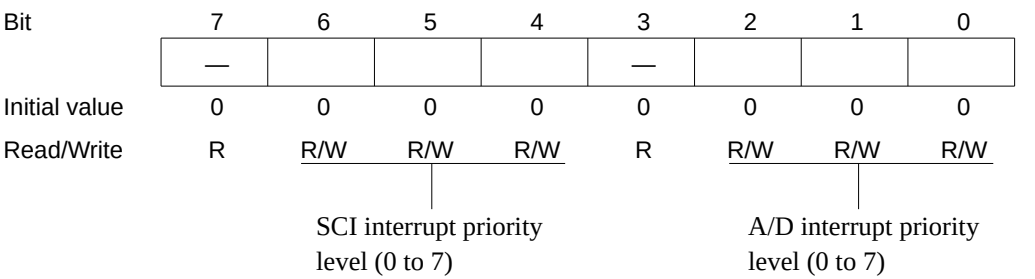
IPRB—Interrupt Priority Register B **H'FFF1** **INTC**



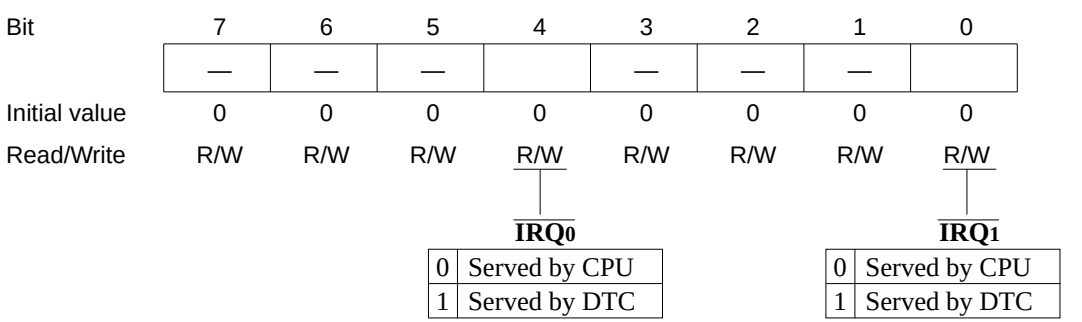
IPRC—Interrupt Priority Register C **H'FFF2** **INTC**

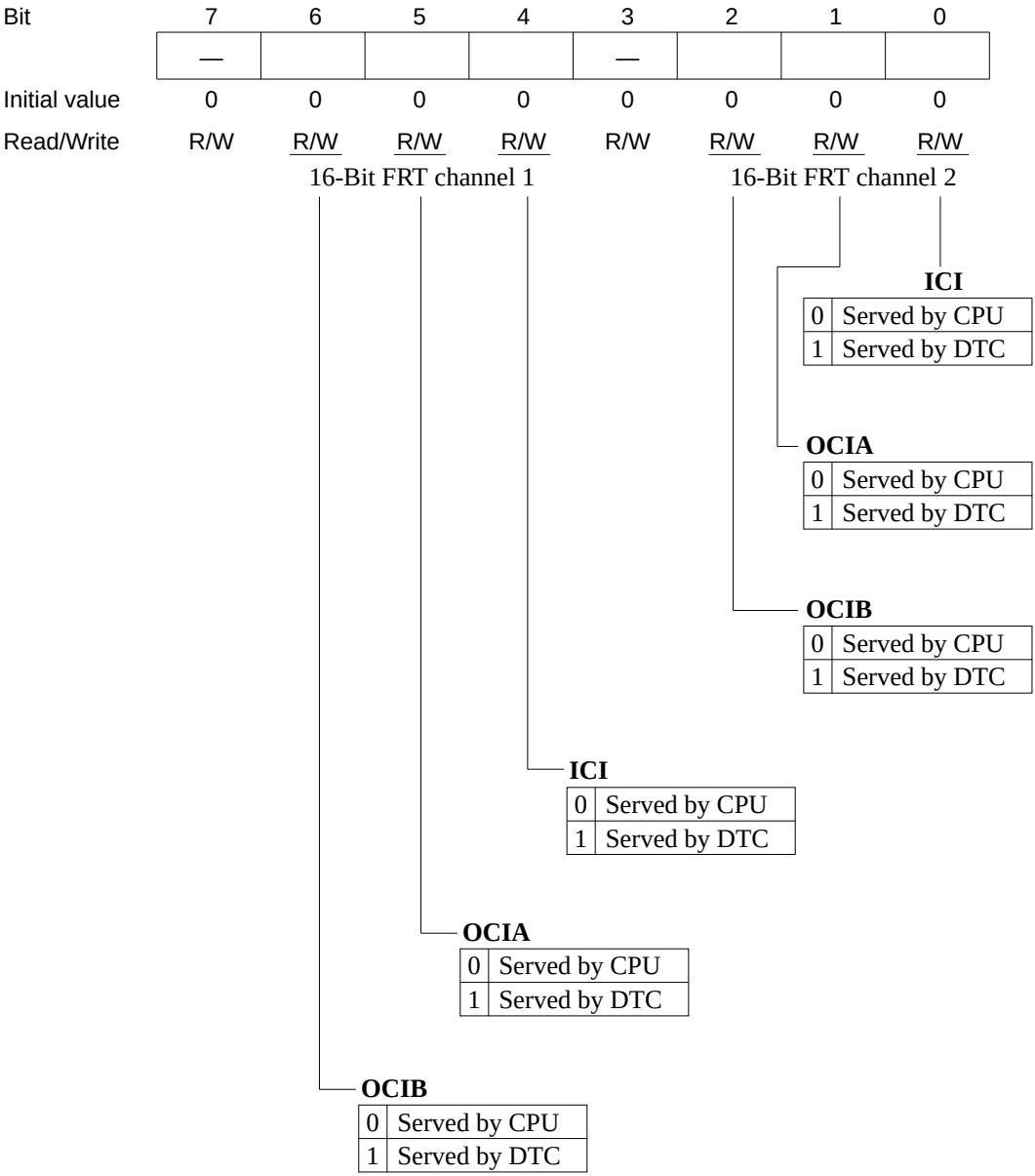


IPRD—Interrupt Priority Register D **H'FFF3** **INTC**

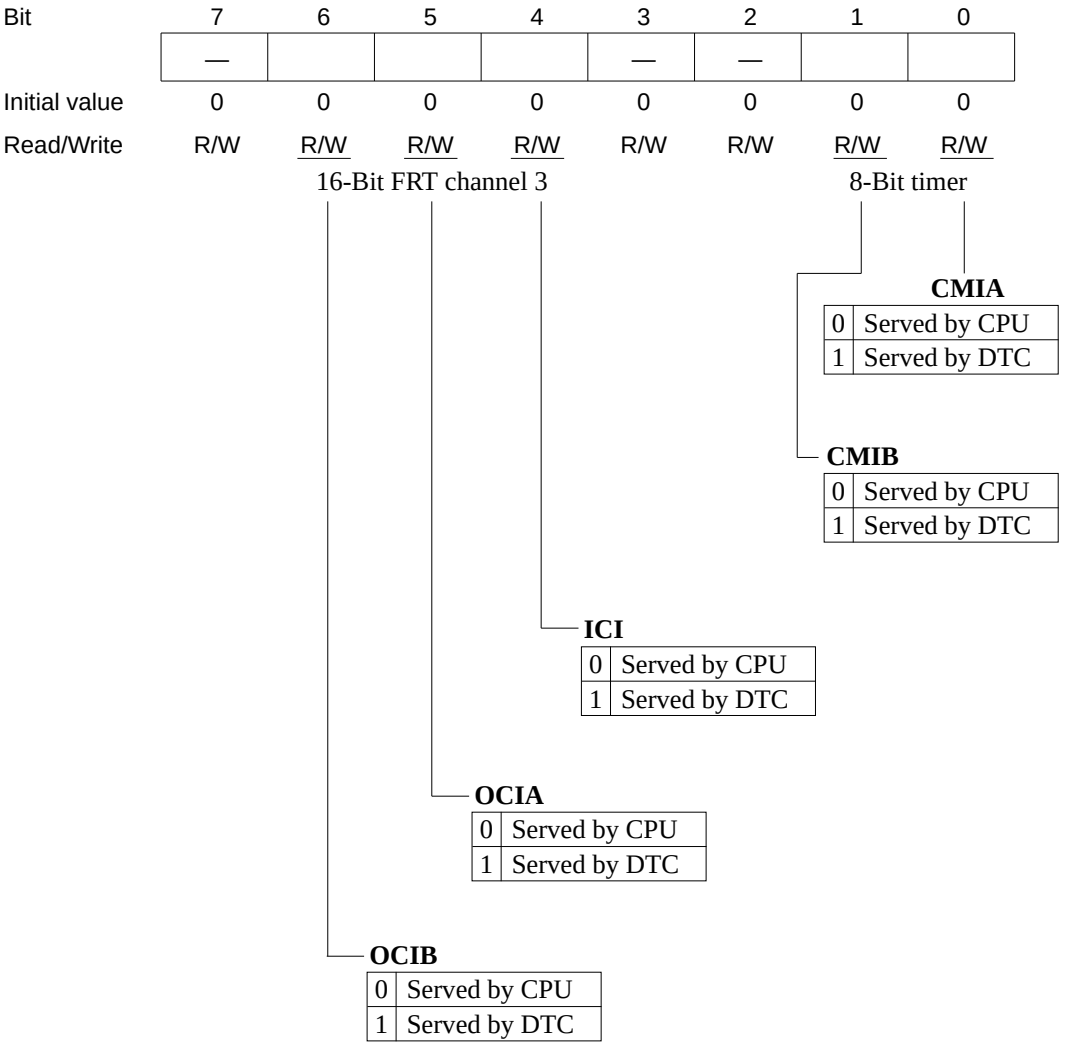


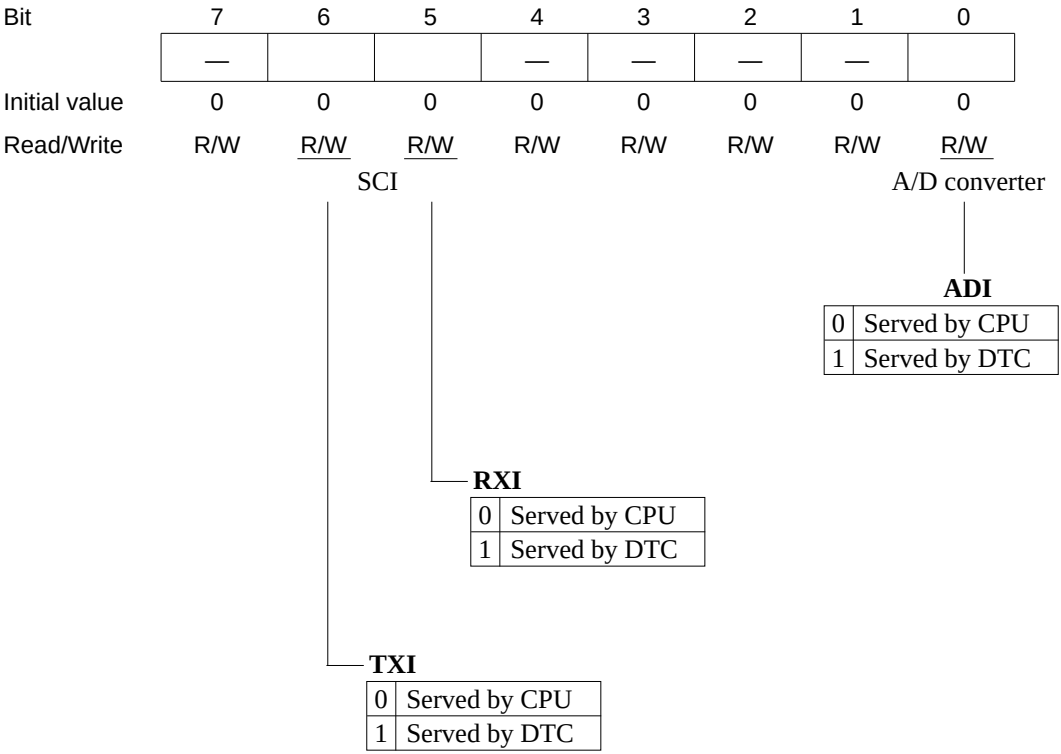
IPRD—Interrupt Priority Register D **H'FFF4** **INTC**




Bit
7
6
5
4
3
2
1
0
—
—
Initial value
0
0
0
0
0
0
0
0
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
16-Bit FRT channel 1
16-Bit FRT channel 2
ICI
0 Served by CPU
1 Served by DTC
OCIA
0 Served by CPU
1 Served by DTC
OCIB
0 Served by CPU
1 Served by DTC
ICI
0 Served by CPU
1 Served by DTC
OCIA
0 Served by CPU
1 Served by DTC
OCIB
0 Served by CPU
1 Served by DTC

DTEC—Data Transfer Enable Register C **H'FFF6** **INTC**




Bit
7
6
5
4
3
2
1
0
—
—
—
—
Initial value
0
0
0
0
0
0
0
0
Read/Write
R/W
R/W
R/W
R/W
R/W
R/W
R/W
R/W
SCI
A/D converter
ADI
0 Served by CPU
1 Served by DTC
RXI
0 Served by CPU
1 Served by DTC
TXI
0 Served by CPU
1 Served by DTC

WCR—Wait-State Control Register **H'FFF8** **WSC**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	WMS1	WMS0	WC1	WC0
Initial value	1	1	1	1	0	0	1	1
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Wait Count 1 and 0

0	0	No wait states (Tw) are inserted.
0	1	1 Wait states are inserted.
1	0	2 Wait states are inserted.
1	1	3 Wait state is inserted.

Wait Mode Select 1 and 0

0	0	Programmable wait mode
0	1	No wait states are inserted, regardless of the wait count.
1	0	Pin wait mode
1	1	Pin auto-wait mode

RAMCR—RAM Control Register **H'FFF9** **RAM**

Bit	7	6	5	4	3	2	1	0
	RAME	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

RAM Enable

0	On-chip RAM is disabled.
1	On-chip RAM is enabled.

MDCR—Mode Control Register **H'FFFA**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	1	1	0	0	0	—*	—*	—*
Read/Write	—	—	—	—	—	R	R	R

Mode Select

Value input at mode pins

* Initialized according to the inputs at pins MD_2, MD_1, and MD_0.

SBYCR—Software Standby Control Register **H'FFFB**

Bit	7	6	5	4	3	2	1	0
	SSBY	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

Software Standby

0	SLEEP instruction causes transition to sleep mode.
1	SLEEP instruction causes transition to software standby mode.