Section 16 RAM

16.1 Overview

The H8/532 includes 1K byte of on-chip static RAM, connected to the CPU by a 16-bit data bus. Both byte and word access to the on-chip RAM are performed in two states, enabling rapid data transfer and instruction execution.

The on-chip RAM is assigned to addresses H'FB80 to H'FF7F in the chip's address space. A RAM control register (RAMCR) can enable or disable the on-chip RAM, permitting these addresses to be allocated to external memory instead, if so desired.

16.1.1 Block Diagram

Figure 16-1 shows the block diagram of the on-chip RAM.

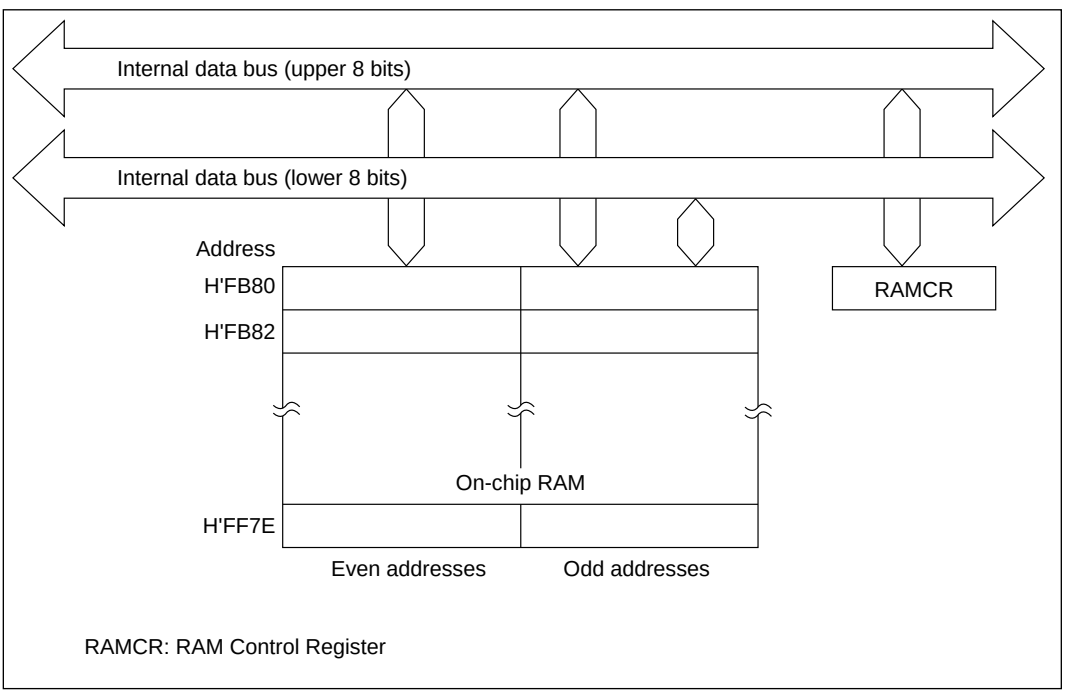

Figure 16-1 Block Diagram of On-Chip RAM

16.1.2 Register Configuration

The on-chip RAM is controlled by the register described in table 16-1.

Table 16-1 RAM Control Register

Name	Abbreviation	R/W	Initial Value	Address
RAM control register	RAMCR	R/W	H'FF	H'FFF9

16.2 RAM Control Register (RAMCR)

Bit	7	6	5	4	3	2	1	0
	RAME	—	—	—	—	—	—	—
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

The RAM control register (RAMCR) is an 8-bit register that enables or disable the on-chip RAM.

Bit 7—RAM Enable (RAME): This bit enables or disables the on-chip RAM.

The RAME bit is initialized on the rising edge of the signal. It is not initialized in the software standby mode.

Bit 7

RAME	Description	
0	On-chip RAM is disabled.	
1	On-chip RAM is enabled.	(Initial value)

Bits 6 to 0—Reserved: These bits cannot be modified and are always read as 1.

16.3 Operation

16.3.1 Expanded Modes (Modes 1, 2, 3, and 4)

If the RAME bit is set to 1, accesses to addresses H'FB80 to H'FF7F are directed to the on-chip RAM. If the RAME bit is cleared to 0, accesses to addresses H'FB80 to H'FF7F are directed to the external data bus.

16.3.2 Single-Chip Mode (Mode 7)

If the RAME bit is set to 1, accesses to addresses H'FB80 to H'FF7F are directed to the on-chip RAM. If the RAME bit is cleared to 0, access of any type (instruction fetch or data read or write) to addresses H'FB80 to H'FF7F causes an address error and initiates the CPU's exception-handling sequence.