Section 12 PWM Timer

12.1 Overview

The H8/532 has an on-chip pulse-width modulation (PWM) timer module with three independent channels (PWM1, PWM2, and PWM3). All three channels are functionally identical. Using an 8-bit timer counter, each PWM channel generates a rectangular output pulse with a duty factor of 0 to 100%. The duty factor is specified in an 8-bit duty register (DTR).

12.1.1 Features

The PWM timer module has the following features:

- Selection of eight clock sources
- Duty factors from 0 to 100% with 1/250 resolution
- Output with positive or negative logic

12.1.2 Block Diagram

Figure 12-1 shows a block diagram of one PWM timer channel.

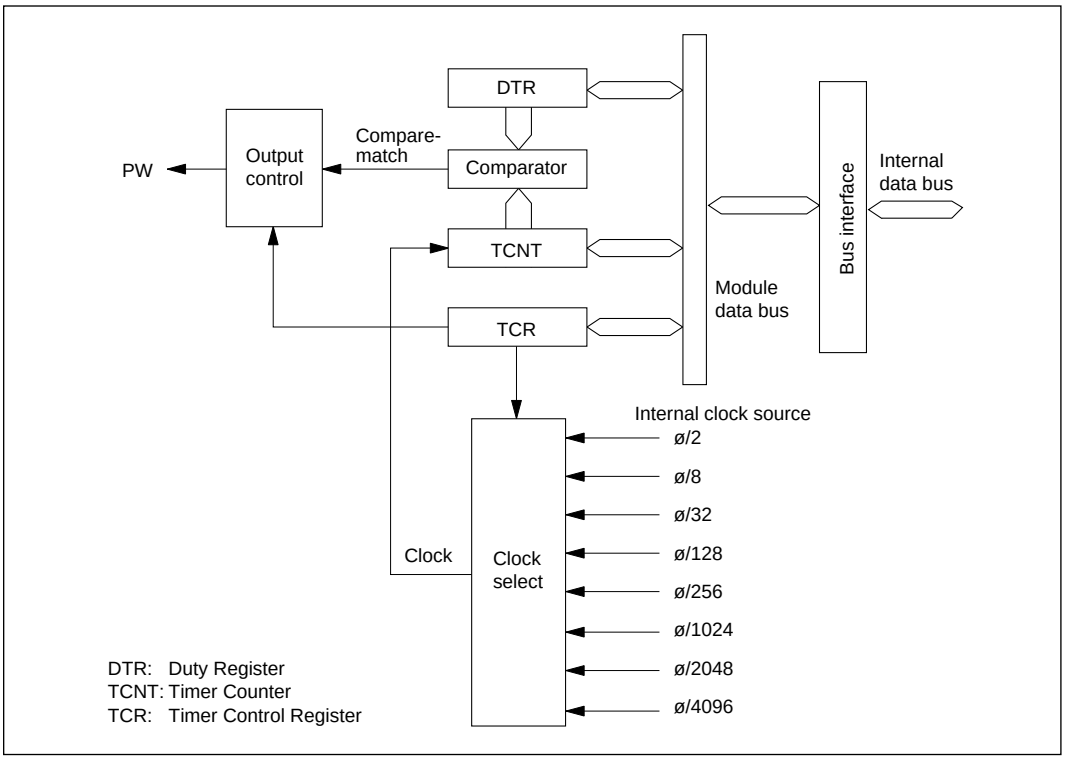


Figure 12-1 Block Diagram of PWM Timer

12.1.3 Input and Output Pins

Table 12-1 lists the output pins of the PWM timer module. There are no input pins.

Table 12-1 Output Pins of PWM Timer Module

Name	Abbreviation	I/O	Function
PWM1 output	PW_1	Output	Pulse output from PWM timer channel 1.
PWM2 output	PW_2	Output	Pulse output from PWM timer channel 2.
PWM3 output	PW_3	Output	Pulse output from PWM timer channel 3.

12.1.4 Register Configuration

The PWM timer module has three registers for each channel as listed in table12-2.

Table 12-2 PWM Timer Registers

Channel	Name	Abbreviation	R/W	Initial Value	Address
1	Timer control register	TCR	R/W	H'38	H'FFC0
	Duty register	DTR	R/W	H'FF	H'FFC1
	Timer counter	TCNT	R/(W)*	H'00	H'FFC2
2	Timer control register	TCR	R/W	H'38	H'FFC4
	Duty register	DTR	R/W	H'FF	H'FFC5
	Timer counter	TCNT	R/(W)*	H'00	H'FFC6
3	Timer control register	TCR	R/W	H'38	H'FFC8
	Duty register	DTR	R/W	H'FF	H'FFC9
	Timer counter	TCNT	R/(W)*	H'00	H'FFCA

* The timer counters are read/write registers, but the write function is for test purposes only. Application programs should never write to these registers.

12.2 Register Descriptions

12.2.1 Timer Counter (TCNT)—H'FFC2, H'FFC4, H'FFCA

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The PWM timer counters (TCNT) are 8-bit up-counters. When the output enable bit (OE) in the timer control register (TCR) is set to 1, the timer counter starts counting pulses of an internal clock source selected by clock select bits 2 to 0 (CKS2 to CKS0). After counting from H'00 to H'F9, the timer counter repeats from H'00.

The PWM timer counters can be read and written, but the write function is for test purposes only. Application software should never write to a PW timer counter, because this may have unpredictable effects.

The PWM timer counters are initialized to H'00 at a reset and in the standby modes, and when the OE bit is cleared to 0.

12.2.2 Duty Register (DTR)—H'FFC1, H'FFC5, H'FFC9

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The duty registers (DTR) specify the duty factor of the output pulse. Any duty factor from 0 to 100% can be selected, with a resolution of 1/250. Writing 0 (H'00) in a DTR gives a 0% duty factor; writing 125 (H'7D) gives a 50% duty factor; writing 250 (H'FA) gives a 100% duty factor.

The timer count is continually compared with the DTR contents. If the DTR value is not 0, when the count increments from H'00 to H'01 the PWM output signal is set to 1. When the count increments to the DTR value, the PWM output returns to 0. If the DTR value is 0 (duty factor 0%), the PWM output remains constant at 0.

The DTRs are double-buffered. A new value written in a DTR while the timer counter is running does not become valid until after the count changes from H'F9 to H'00. When the timer counter is stopped (while the OE bit is 0), new values become valid as soon as written. When a DTR is read, the value read is the currently valid value.

The DTRs are initialized to H'FF at a reset and in the standby modes.

12.2.3 Timer Control Register (TCR)—H'FFC0, H'FFC4, H'FFC8

Bit	7	6	5	4	3	2	1	0
	OE	OS	—	—	—	CKS2	CKS1	CKS0
Initial value	0	0	1	1	1	0	0	0
Read/Write	R/W	R/W	—	—	—	R/W	R/W	R/W

The TCRs are 8-bit readable/writable registers that select the clock source and control the PWM outputs.

The TCRs are initialized to H'38 at a reset and in the standby modes.

Bit 7—Output Enable (OE): This bit enables the timer counter and the PWM output.

Bit 7 OE	Description
0	PWM output is disabled. TCNT is cleared to H'00 and stopped. (Initial value)
1	PWM output is enabled. TCNT runs.

Bit 6—Output Select (OS): This bit selects positive or negative logic for the PWM output.

Bit 6 OS	Description
0	Positive logic; positive-going PWM pulse, 1 = High (Initial value)
1	Negative logic; negative-going PWM pulse, 1 = Low

Bits 5 to 3—Reserved: These bits cannot be modified and are always read as 1.

Bits 2, 1, and 0—Clock Select (CKS2, CKS1, and CKS0): These bits select one of eight clock sources obtained by dividing the system clock (ø).

Bit 2 CKS2	Bit 1 CKS1	Bit 0 CKS0	Description
0	0	0	ø/2 (Initial value)
0	0	1	ø/8
0	1	0	ø/32
0	1	1	ø/128
1	0	0	ø/256
1	0	1	ø/1024
1	1	0	ø/2048
1	1	1	ø/4096

From the clock source frequency, the resolution, period, and frequency of the PWM output can be calculated as follows.

Resolution = 1/clock source frequency
PWM period = resolution × 250
PWM frequency = 1/PWM period

If the ø clock frequency is 10MHz, then the resolution, period, and frequency of the PWM output for each clock source are given in table12-3.

Table 12-3 PWM Timer Parameters for 10MHz System Clock

Internal Clock Frequency	Resolution	PWM Period	PWM Frequency
ø/2	200ns	50µs	20kHz
ø/8	800ns	200µs	5kHz
ø/32	3.2µs	800µs	1.25kHz
ø/128	12.8µs	3.2ms	312.5Hz
ø/256	25.6µs	6.4ms	156.3Hz
ø/1024	102.4µs	25.6ms	39.1Hz
ø/2048	204.8µs	51.2ms	19.5Hz
ø/4096	409.6µs	102.4ms	9.8Hz

12.3 Operation

Figure 12-2 shows the timing of the PWM timer operation.

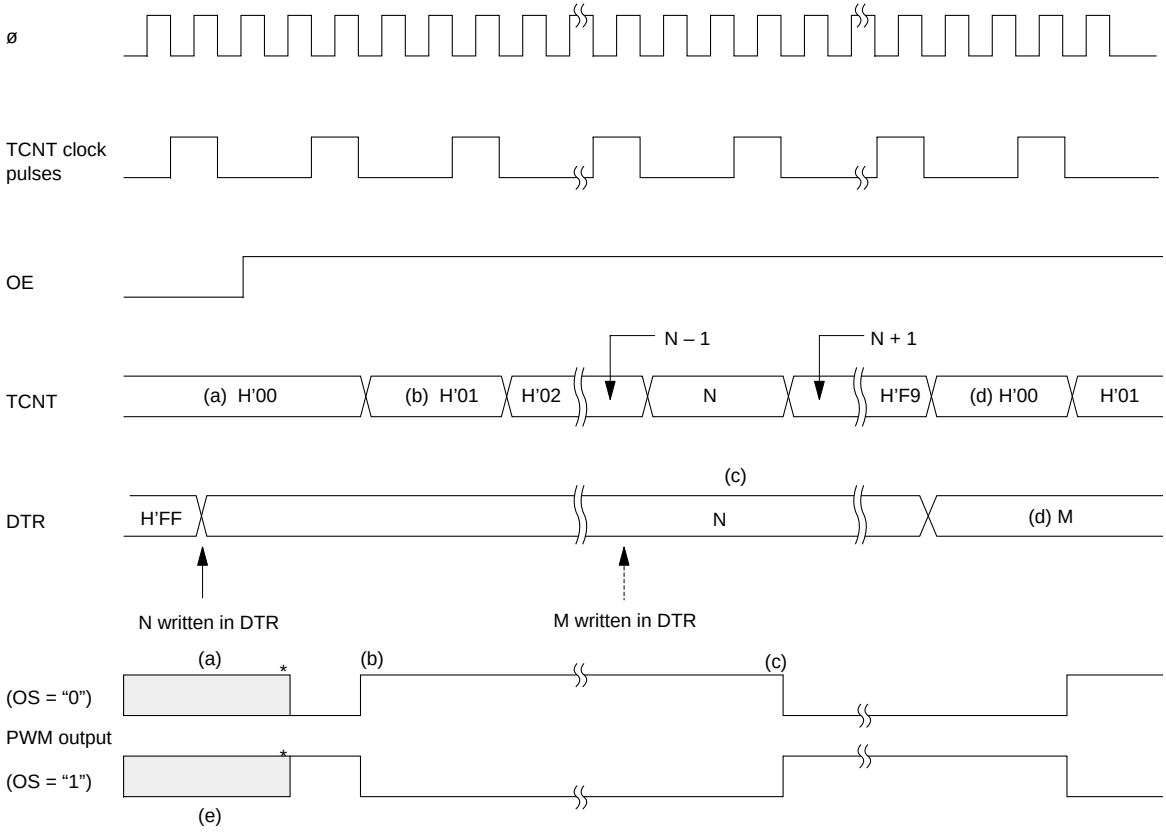
1. Positive Logic (OS = "0")

(1) When OE = "0"—(a) in figure 12-2: The timer count is held at H'00 and PWM output is inhibited. (The pin is used for port 9 input/output, and its state depends on the corresponding port 9 data register and data direction register.) Any value (such as N in figure 12-2) written in the DTR becomes valid immediately.

(2) When OE = "1"

i) The timer counter begins incrementing, and the PWM output goes High. [(b) in figure 12-2]
ii) When the count reaches the DTR value, the PWM output goes Low. [(c) in figure 12-2]
iii) If the DTR value is changed (by writing the data "M" in figure 12-2), the new value becomes valid after the timer count changes from H'F9 to H'00. [(d) in figure 12-2]

2. Negative Logic (OS = "1"): The operation is the same except that High and Low are reversed in the PWM output. [(e) in figure 12-2]



* Used for port 9 input/output: state depends on values in data register and data direction register.

Figure 12-2 PWM Timing

12.4 Application Notes

Two notes on the use of the PWM timer module are given below.

1. Any necessary changes to the clock select bits (CKS2 to CKS0) and output select bit (OS) should be made before the output enable bit (OE) is set to 1.
2. If the DTR value is H'00, the duty factor is 0% and PWM output remains constant at 0. If the DTR value is H'FA to H'FF, the duty factor is 100% and PWM output remains constant at 1. (For positive logic, 0 is Low and 1 is High. For negative logic, 0 is High and 1 is Low.)