Appendix E Pin State

E.1 Port State of Each Pin State

Table E-1 Port State

Port Pin Name	Mode	Reset	Hardware Standby Mode	Software Standby mode	Sleep Mode	Bus-right Release Mode	Program Execution State (Normal Operation)
$P1_7$ to $P1_2$	1						Input/Output port or
TMO, $\overline{IRQ_1}$, $\overline{IRQ_0}$	2						Control signal Input/
$\overline{WAIT}$, $\overline{BREQ}$,	3	T	T	keep*1	keep*3	keep*4	Output
$\overline{BACK}$	4						
	7			keep*2	keep	---	Input/Output port
$P1_1$/E	1			(DDR = 1)	(DDR = 1)	(DDR = 1)	(DDR = 1)
$P1_0$/ø	2	Clock		ø = H	Clock output	Clock output	Clock output
	3	output	T	E = L	(DDR = 0)	(DDR = 0)	(DDR = 0)
	4			(DDR = 0)	T	T	Input port
	7			T		---	
$P2_4$ to $P2_0$	1						$\overline{WR}$, $\overline{RD}$, $\overline{DS}$,
$\overline{WR}$, $\overline{RD}$, $\overline{DS}$,	2	H		T	H	T	R/$\overline{W}$, $\overline{AS}$
R/$\overline{W}$, $\overline{AS}$	3						
	4						
	7	T		keep	keep	---	Input/Output port
$P3_7$ to $P3_0$	1						
D_7 to D_0	2			T	T	T	D_7 to D_0
	3	T	T				
	4						
	7			keep	keep	---	Input/Output port
$P4_7$ to $P4_0$	1						
A_7 to A_0	2	L		T	L	T	A_7 to A_0
	3		T				
	4						
	7	T		keep	keep	---	Input/Output port
$P5_7$ to $P5_0$	1	L		T	L	T'	A_{15} to A_8
A_{15} to A_8	2	T		T*6	*5	T*6	Address/Input port
	3	L	T	T	L	T	A_{15} to A_8
	4	T		T*6	*5	T*6	Address/Input port
	7			keep	keep	---	Input/Output port

Table E-1 Port State (cont)

Port Pin Name	Mode	Reset	Hardware Standby Mode	Software Standby mode	Sleep Mode	Bus-right Release Mode	Program Execution State (Normal Operation)
$P6_3$ to $P6_0$	1			keep	keep	keep	Input/Output port
A_{19} to A_{16}	2	T					
	3	L	T	T	L	T	A_{19} to A_{16}
	4	T		T*6	*5	T*6	Address/Input port
	7			keep	keep	---	Input/Output port
$P7_7$ to $P7_0$	1						
	2						
	3	T	T	keep*2	keep	keep	Input port
	4						
	7						
$P8_7$ to $P8_0$	1						
	2						
	3	T	T	T	T	T	Input port
	4						
	7						
$P9_7$ to $P9_0$	1						
	2						
	3	T	T	keep*2	keep	keep	Input/Output port
	4						
	7						

H: “High” = High level

L: “Low” = Low level

T: High Impedance

keep: If DDR = 0 and DR = 1 in port 5 and 6, Pull-up MOS holds on-state.

Notes:

*1 8 Bit Timer is reset, so $P1_7$ becomes input or output port controlled by DDR and DR. Also $P1_2$ goes to the high impedance state when it is programmed as $\overline{BACK}$ output.

*2 On-chip supporting modules are reset. So these pins become input or output ports controlled by DDR and DR.

*3 $\overline{BREQ}$ can be accepted and $\overline{BACK}$ goes LOW.

*4 $\overline{BACK}$ outputs LOW.

*5 The pins programmed as address bus output LOW and others programmed as input are at the high impedance state.
If DDR = 0 and DR = 1, the pull-up MOS’s keep ON state.

*6 If DDR = 0 and DR = 1, the pull-up MOS’s keep ON state.

Table E-2 Pull-Up MOS State

Port	Mode	Reset	Hardware Standby Mode	Other Operating State*
$P5_7$ to $P5_0$ A_{15} to A_8	1	OFF	OFF	OFF
	2			ON/OFF
	3			OFF
	4			ON/OFF
	7			
$P5_7$ to $P5_0$ A_{15} to A_8	1	OFF	OFF	ON/OFF
	2			
	3			OFF
	4			ON/OFF
	7			

OFF: Pull-up MOS is always OFF.

ON/OFF: Pull-up MOS holds on-state only when DDR = “0” and DR = 1.

* Including Software Standby Mode

E.2 Pin Status in the Reset State

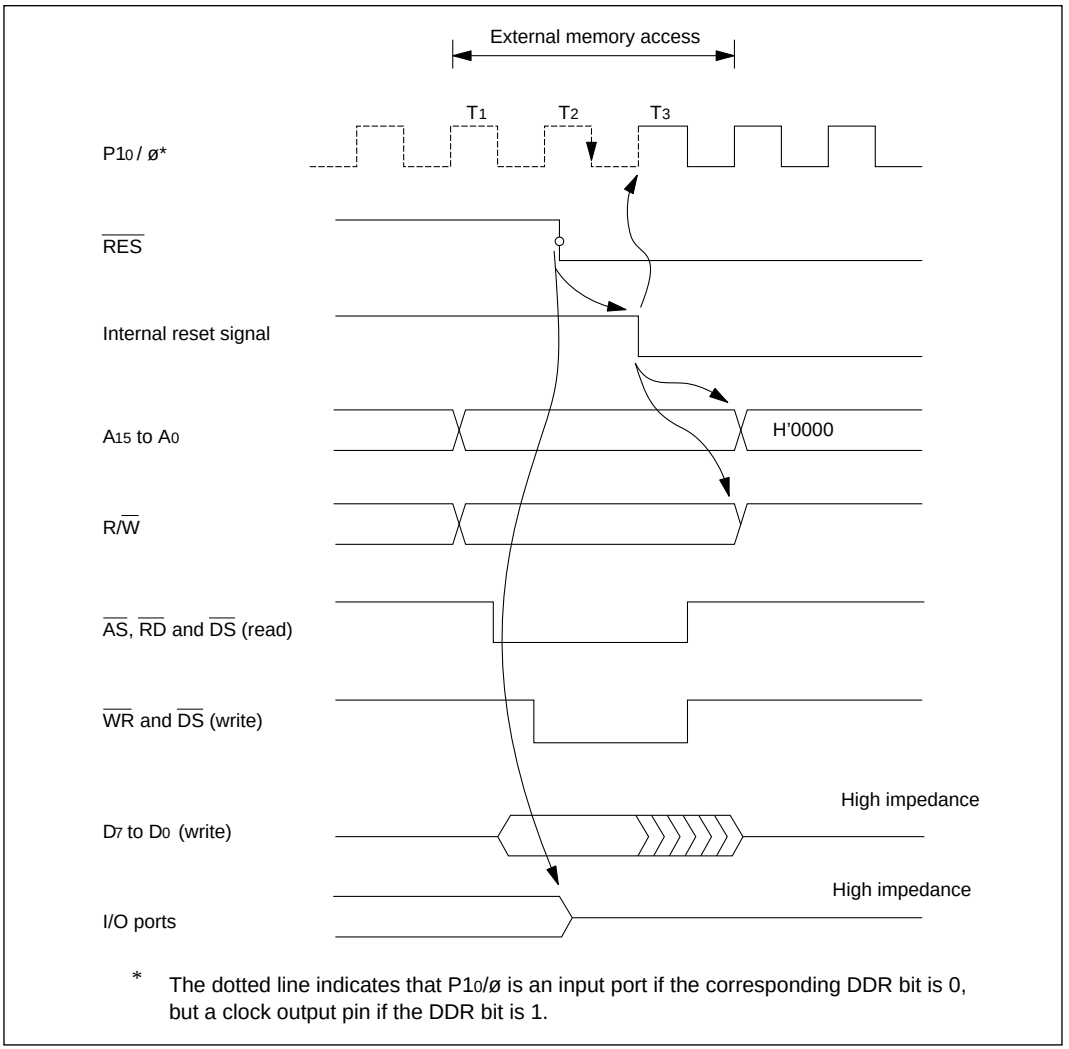
1. Mode 1

Figures E-1 and E-2 show how the pin states change when the $\overline{\text{RES}}$ pin goes Low during external memory access in mode 1.

As soon as $\overline{\text{RES}}$ goes Low, all ports are initialized to the input (high-impedance) state. The $\overline{\text{AS}}$, $\overline{\text{DS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ signals all go High. The data bus (D_7 to D_0) is placed in the high-impedance state.

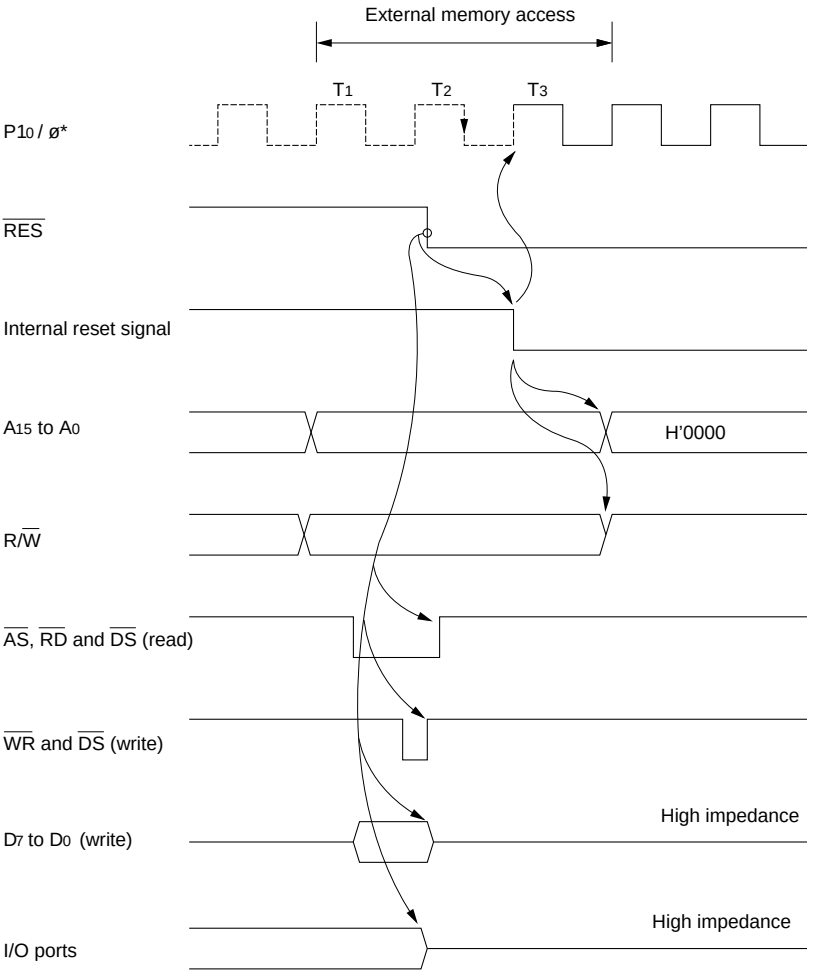
The address bus and the R/$\overline{\text{W}}$ signal are initialized 1.5 ø clock periods after the Low state of the $\overline{\text{RES}}$ pin is sampled. All address bus signals are made Low. The R/$\overline{\text{W}}$ signal is made High.

The clock output pins $P1_0$/ø and $P1_1$/E are initialized 0.5 ø clock periods after the Low state of the $\overline{\text{RES}}$ pin is sampled. Both pins are initialized to the output state.



* The dotted line indicates that P1$_0$/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-1 Reset during Memory Access (Mode 1)



* The dotted line indicates that P1$_0$/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-2 Reset during Memory Access (Mode 1)

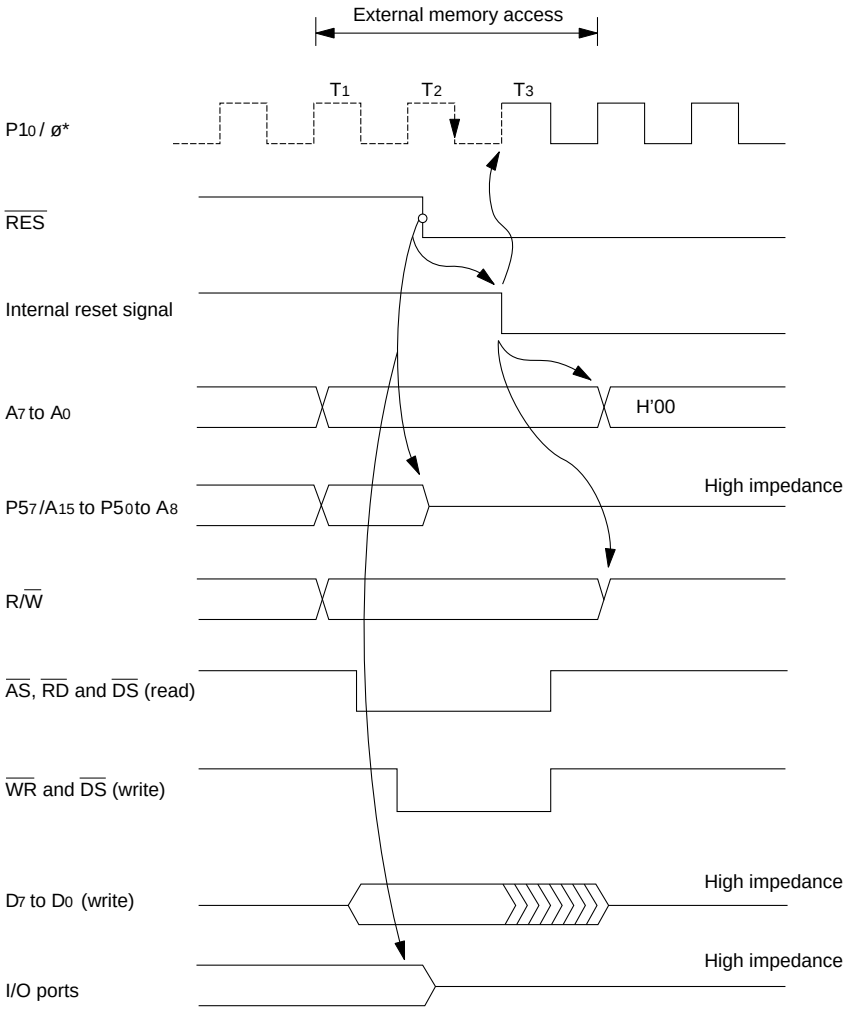
2. Mode 2

Figures E-3 and E-4 show how the pin states change when the $\overline{RES}$ pin goes Low during external memory access in mode 2.

As soon as $\overline{RES}$ goes Low, all ports are initialized to the input (high-impedance) state. The $\overline{AS}$, $\overline{DS}$, $\overline{RD}$, and $\overline{WR}$ signals all go High. The data bus (D_7 to D_0) is placed in the high-impedance state. Pins $P5_7/A_{15}$ to $P5_0/A_8$ of the address bus are initialized as input ports.

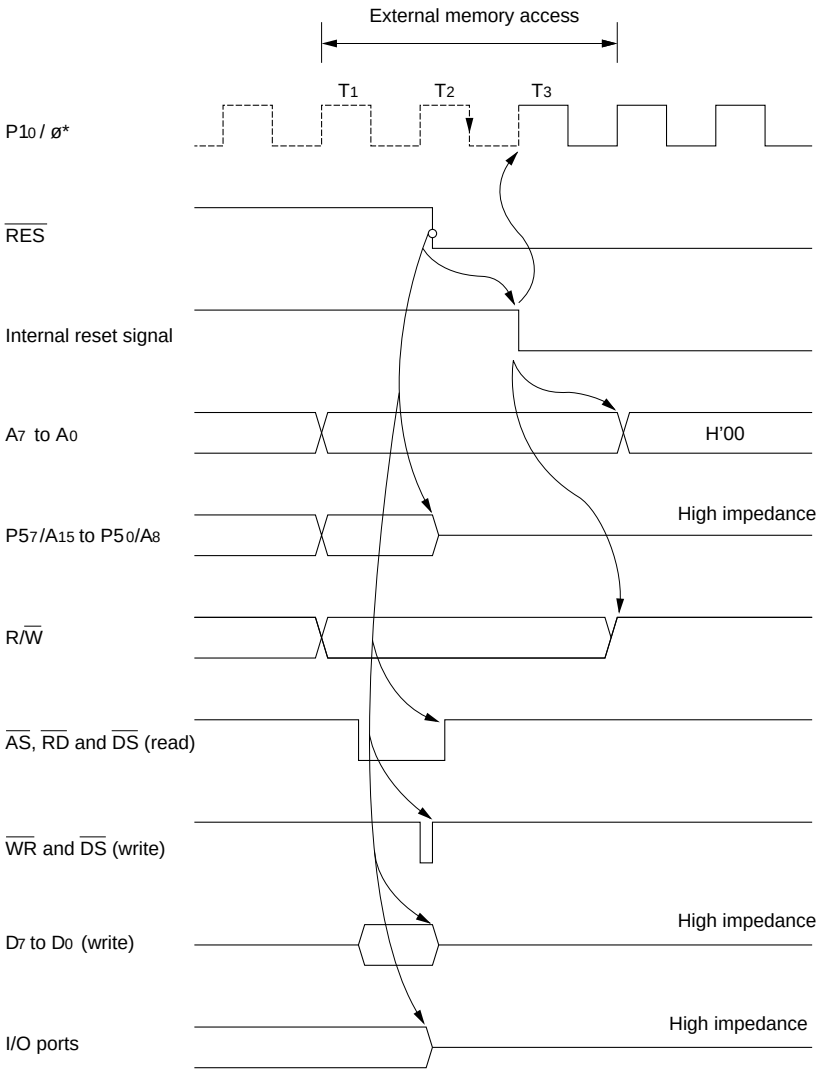
Pins A_7 to A_0 of the address bus and the $R/\overline{W}$ signal are initialized 1.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. Pins A_7 to A_0 are made Low. The signal is made High.

The clock output pins $P1_0$/ø and $P1_1$/E are initialized 0.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. Both pins are initialized to the output state.



* The dotted line indicates that P10/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-3 Reset during Memory Access (Mode 2)



* The dotted line indicates that P10/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-4 Reset during Memory Access (Mode 2)

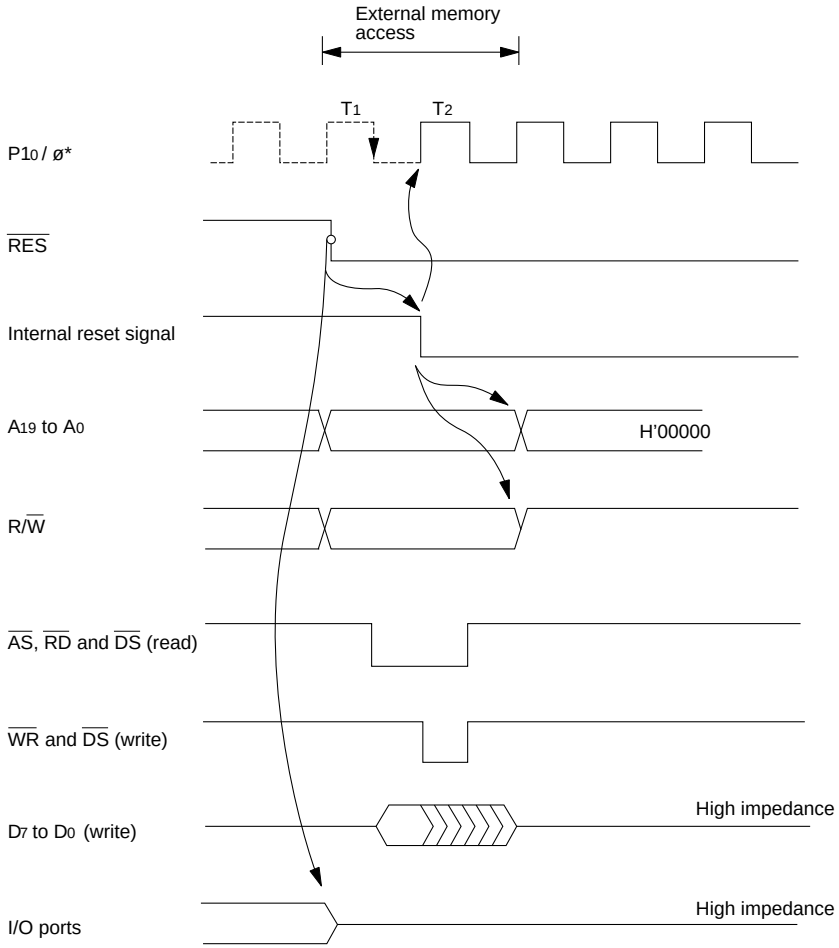
3. Mode 3

Figures E-5 and E-6 show how the pin states change when the $\overline{RES}$ pin goes Low during external memory access in mode 3.

As soon as $\overline{RES}$ goes Low, all ports are initialized to the input (high-impedance) state. The $\overline{AS}$, $\overline{DS}$, $\overline{RD}$, and $\overline{WR}$ signals all go High. The data bus (D_7 to D_0) is placed in the high-impedance state.

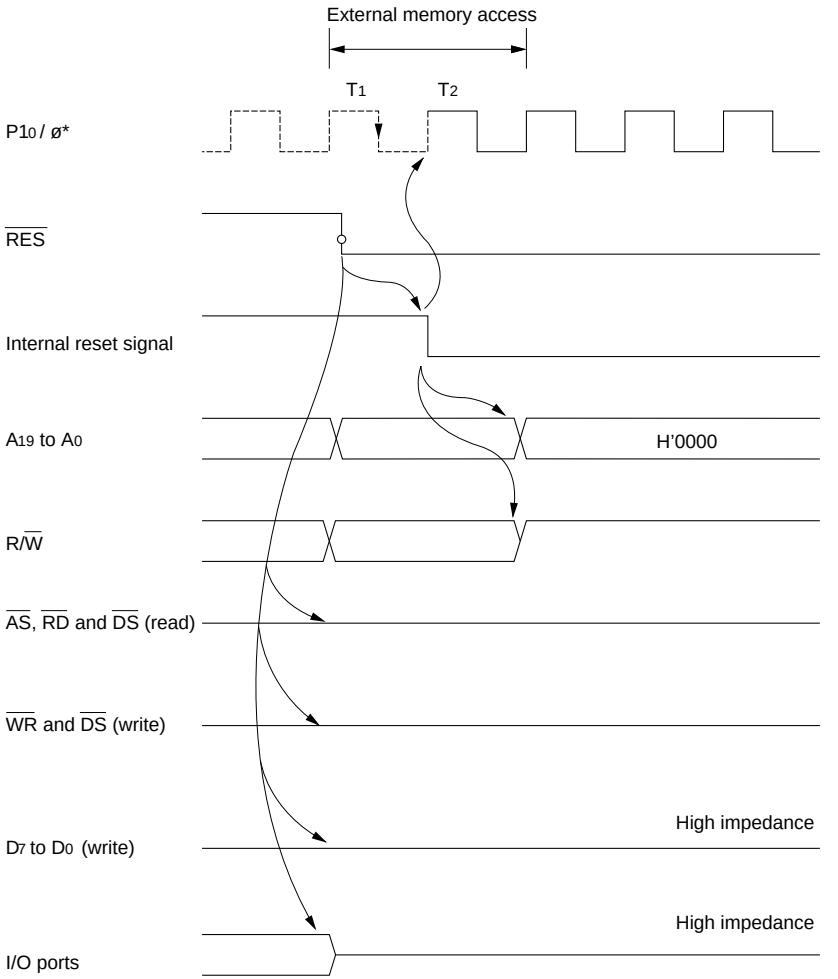
The address bus and the signal are initialized 1.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. All address bus signals are made Low. The R/$\overline{W}$ signal is made High.

The clock output pins $P1_0$/ø and $P1_1$/E are initialized 0.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. Both pins are initialized to the output state.



* The dotted line indicates that P1₀/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-5 Reset during Memory Access (Mode 3)



* The dotted line indicates that P1$_0$/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-6 Reset during Memory Access (Mode 3)

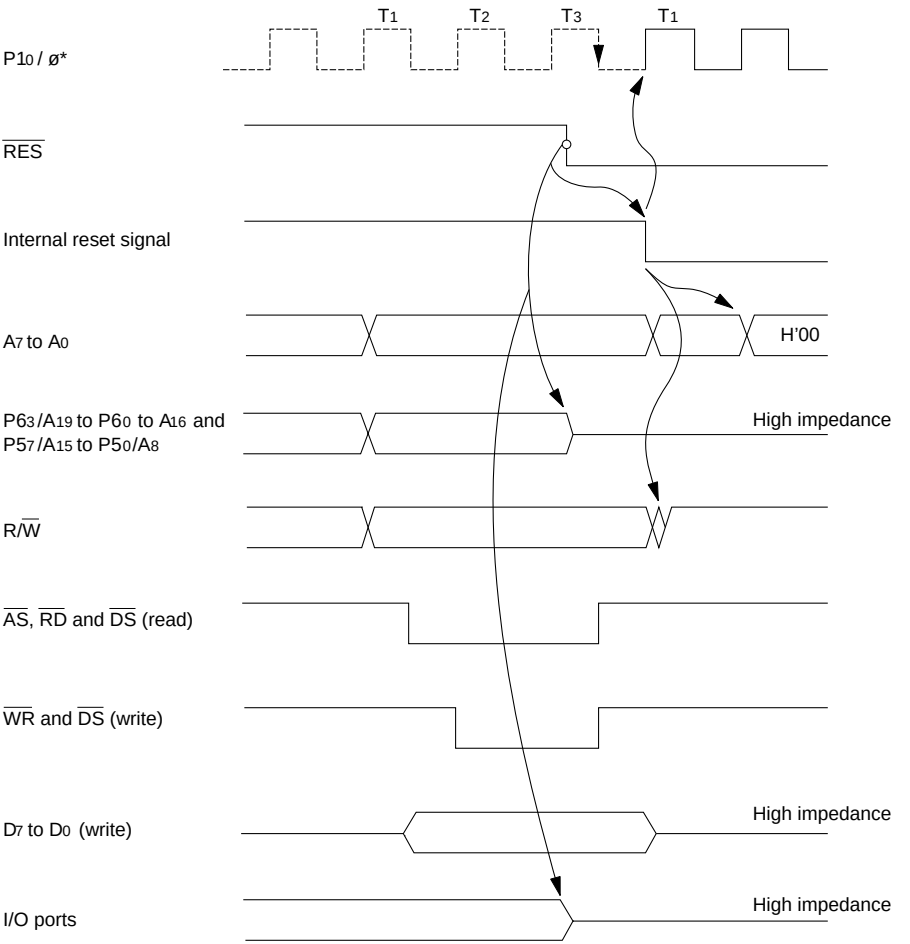
4. Mode 4

Figures E-7 and E-8 show how the pin states change when the $\overline{RES}$ pin goes Low during external memory access in mode 4.

As soon as $\overline{RES}$ goes Low, all ports are initialized to the input (high-impedance) state. The $\overline{AS}$, $\overline{DS}$, $\overline{RD}$, and $\overline{WR}$ signals all go High. The data bus (D_7 to D_0) is placed in the high-impedance state. Pins $P5_7/A_{15}$ to $P5_0/A_8$ of the address bus and pins $P6_3/A_{19}$ to $P6_0/A_{16}$ of the page address bus are initialized as input ports.

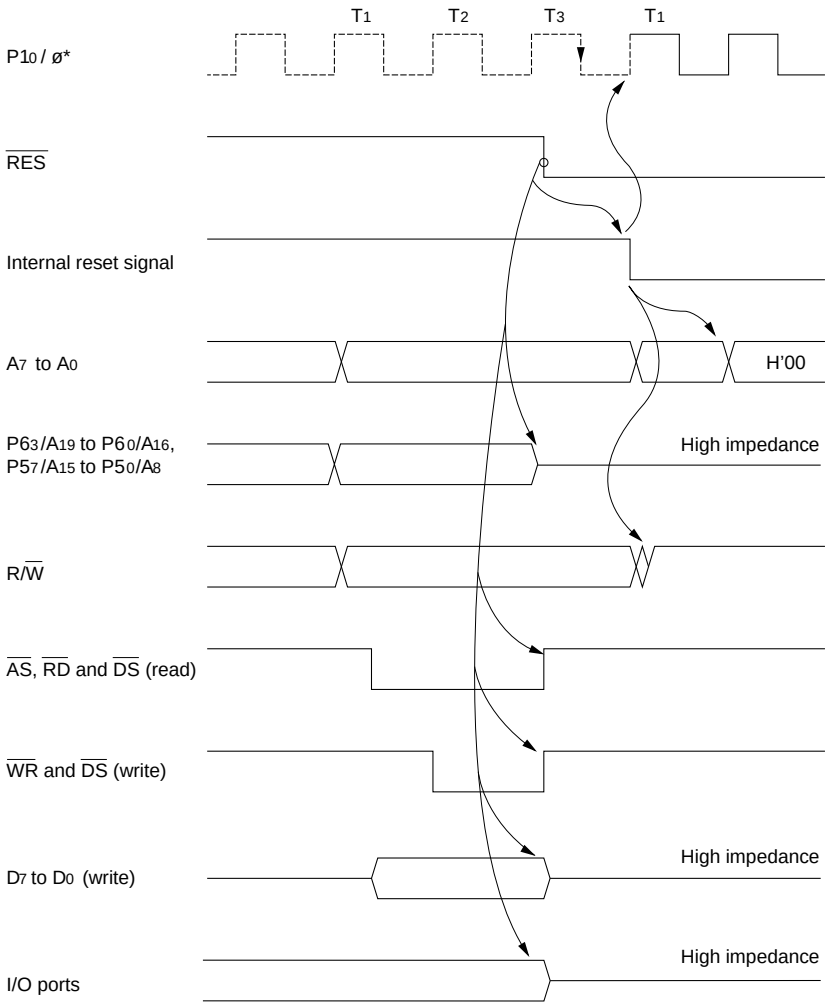
Pins A_7 to A_0 of the address bus and the R/$\overline{W}$ signal are initialized 1.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. Pins A_7 to A_0 are made Low. The R/$\overline{W}$ signal is made High.

The clock output pins $P1_0$/ø and $P1_1$/E are initialized 0.5 ø clock periods after the Low state of the $\overline{RES}$ pin is sampled. Both pins are initialized to the output state.



* The dotted line indicates that P10/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-7 Reset during Memory Access (Mode 4)



* The dotted line indicates that P1$_0$/ø is an input port if the corresponding DDR bit is 0, but a clock output pin if the DDR bit is 1.

Figure E-8 Reset during Memory Access (Mode 4)

5. Mode 7

Figures E-9 and E-10 show how the pin states change when the $\overline{\text{RES}}$ pin goes Low in mode 7.

As soon as $\overline{\text{RES}}$ goes Low, all ports are initialized to the input (high-impedance) state.

The clock output pins P10/ø and P11/E are initialized 0.5 ø clock periods after the Low state of the $\overline{\text{RES}}$ pin is sampled. Both pins are initialized to the output state.

ZTAT Versions

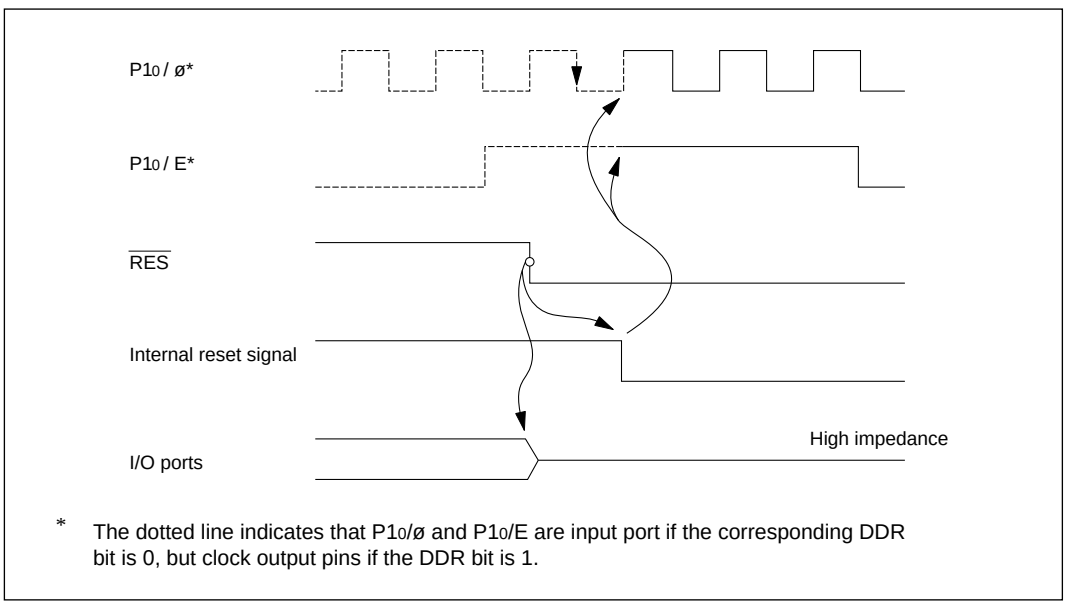
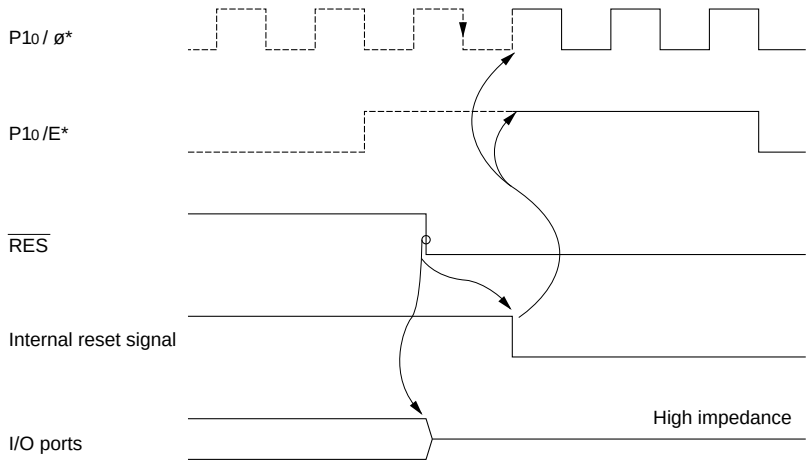


Figure E-9 Reset during Memory Access (Mode 7)



* The dotted line indicates that P1₀/ø and P1₀/E are input port if the corresponding DDR bit is 0, but clock output pins if the DDR bit is 1.

Figure E-10 Reset during Memory Access (Mode 7)