Section 1 Overview

1.1 Features

The H8/532 is an original Hitachi CMOS microcomputer unit (MCU) comprising a high-performance CPU core plus a full range of supporting functions—an entire system integrated onto a single chip.

The CPU features a highly orthogonal instruction set that permits addressing modes and data sizes to be specified independently in each instruction. An internal 16-bit architecture and 16-bit access to on-chip memory enhance the CPU's data-processing capability and provide the speed needed for realtime control applications.

The on-chip supporting functions include RAM, ROM, timers, a serial communication interface (SCI), A/D conversion, and I/O ports. An on-chip data transfer controller (DTC) can transfer data in either direction between memory and I/O independently of the CPU.

For the on-chip ROM, a choice is offered between masked ROM and programmable ROM (PROM). The PROM version can be programmed by the user with a general-purpose PROM writer.

Table 1-1 lists the main features of the H8/532 chip.

Table 1-1 Features

Feature	Description
CPU	General-register machine • Eight 16-bit general registers • Five 8-bit and two 16-bit control registers High speed • Maximum clock rate: 10MHz (oscillator frequency: 20MHz) Expanded operating modes supporting external memory • Minimum mode: up to 64K-byte address space • Maximum mode: up to 1M-byte address space Highly orthogonal instruction set • Addressing modes and data size can be specified independently for each instruction 1.5 Addressing modes • Register-register operations • Register-memory operations Instruction set optimized for C language • Special short formats for frequently-used instructions and addressing modes
Memory	• 1K-Byte high-speed RAM on-chip • 32K-Byte programmable or masked ROM on-chip
16-Bit free-running timer (FRT) (3 channels)	Each channel provides: • 1 free-running counter (which can count external events) • 2 output-compare registers • 1 input capture register
8-Bit timer (1 channel)	• One 8-bit up-counter (which can count external events) • 2 time constant registers
PWM timer (3 channels)	• Generates pulses with any duty ratio from 0 to 100% • Resolution: 1/250
Watchdog timer (WDT) (1 channel)	• An overflow generates a nonmaskable interrupt • Can also be used as an interval timer

Table 1-1 Features (cont)

Feature	Description
Serial communication interface (SCI)	• Asynchronous or synchronous mode (selectable) • Full duplex: can send and receive simultaneously • Built-in baud rate generator
A/D converter	• 10-Bit resolution • 8 channels, controllable in single mode or scan mode (selectable) • Sample-and-hold function
I/O ports	• 57 Input/output pins (six 8-bit ports, one 5-bit port, one 4-bit port) • 8 Input-only pins (one 8-bit port) • Memory-mapped I/O
Interrupt controller (INTC)	• 3 external interrupt pins (NMI, $\overline{IRQ_0}$, $\overline{IRQ_1}$) • 19 internal interrupts • 8 priority levels
Data transfer controller (DTC)	Performs bidirectional data transfer between memory and I/O independently of the CPU
Wait-state controller (WSC)	Can insert wait states in access to external memory or I/O
Operating modes	5 MCU operating modes • Expanded minimum modes, supporting up to 64k bytes external memory with or without using on-chip ROM (Modes 1 and 2) • Expanded maximum modes, supporting up to 1M byte external memory with or without using on-chip ROM (Modes 3 and 4) • Single-chip mode (Mode 7) 3 power-down modes • Sleep mode • Software standby mode • Hardware standby mode
Other features	• E clock output available • Clock generator on-chip

Model Name	Package Options	ROM
HD6475328CG	84-Pin windowed LCC (CG-84)	PROM
HD6475328CP	84-Pin PLCC (CP-84)	
HD6475328F	80-Pin QFP (FP-80A)	
HD6435328CP	84-Pin PLCC (CP-84)	Mask
HD6435328F	80-Pin QFP (FP-80A)	ROM

1.2 Block Diagram

Figure 1-1 shows a block diagram of the H8/532 chip.

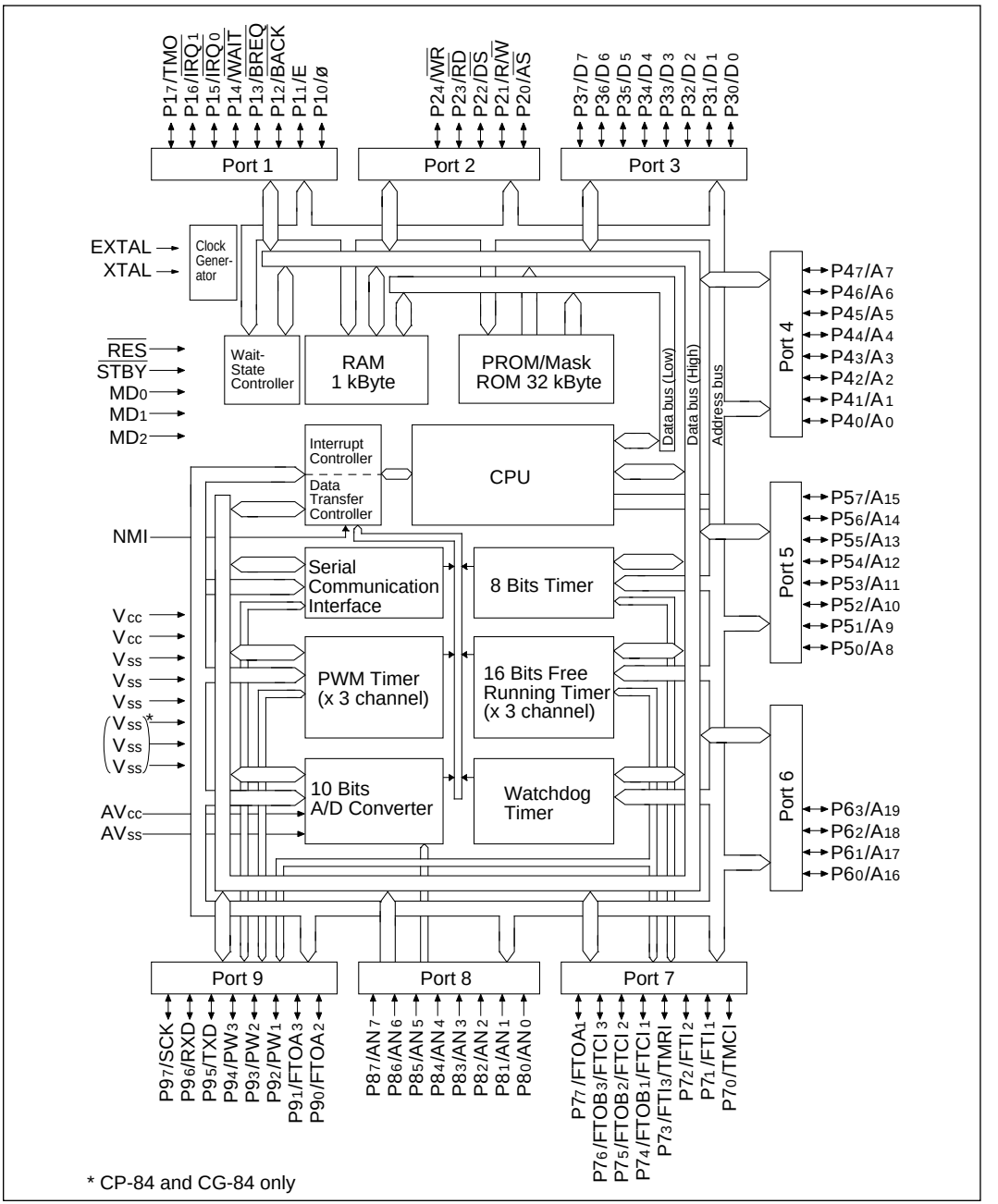

Figure 1-1 Block Diagram

1.3 Pin Arrangements and Functions

1.3.1 Pin Arrangement

Figure 1-2 shows the pin arrangement of the CP-84 package. Figure 1-3 shows the pin arrangement of the CG-84 package. Figure 1-4 shows the pin arrangement of the FP-80A package.

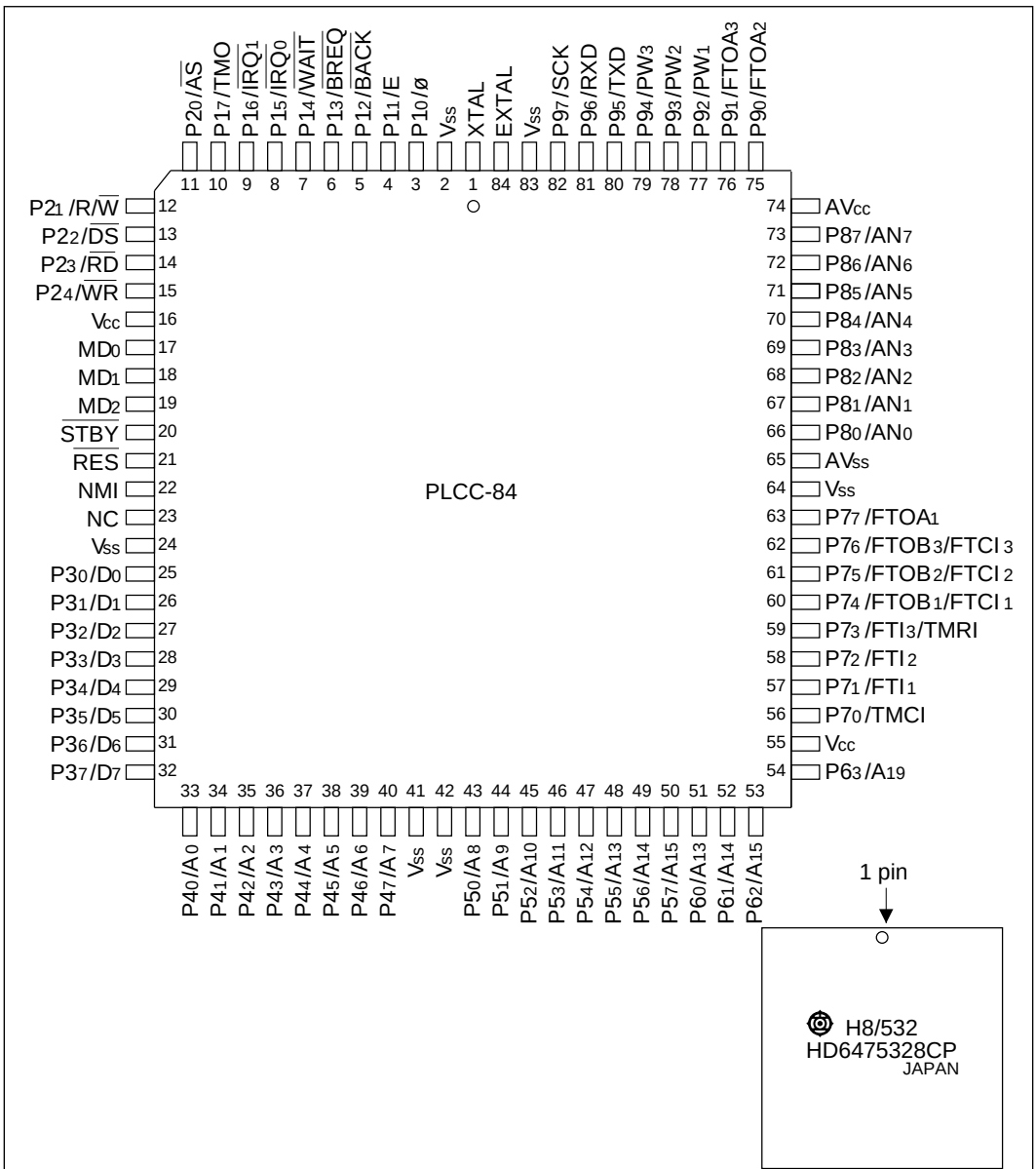

Figure 1-2 Pin Arrangement (CP-84, Top View)

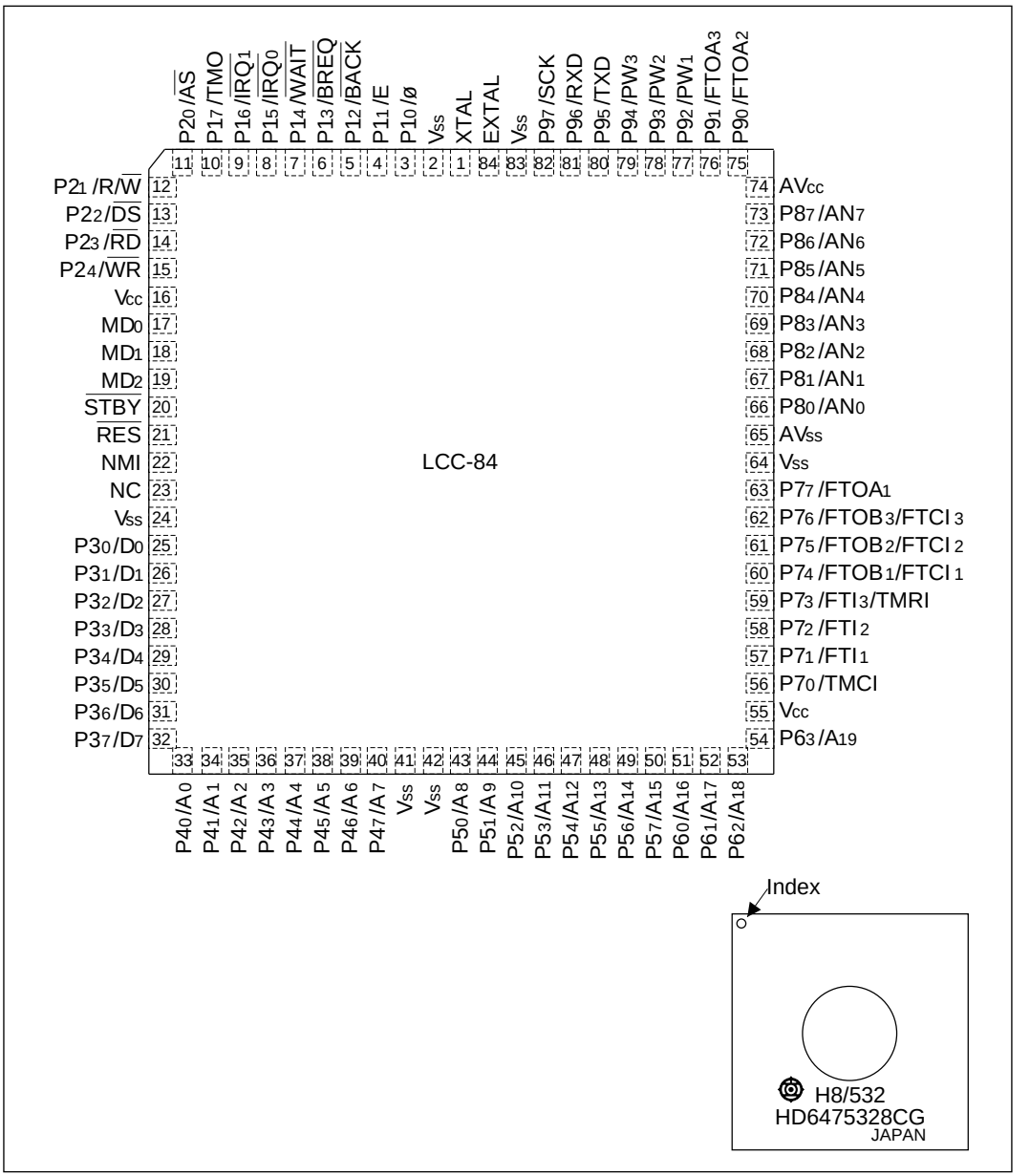

Figure 1-3 Pin Arrangement (CG-84, Top View)

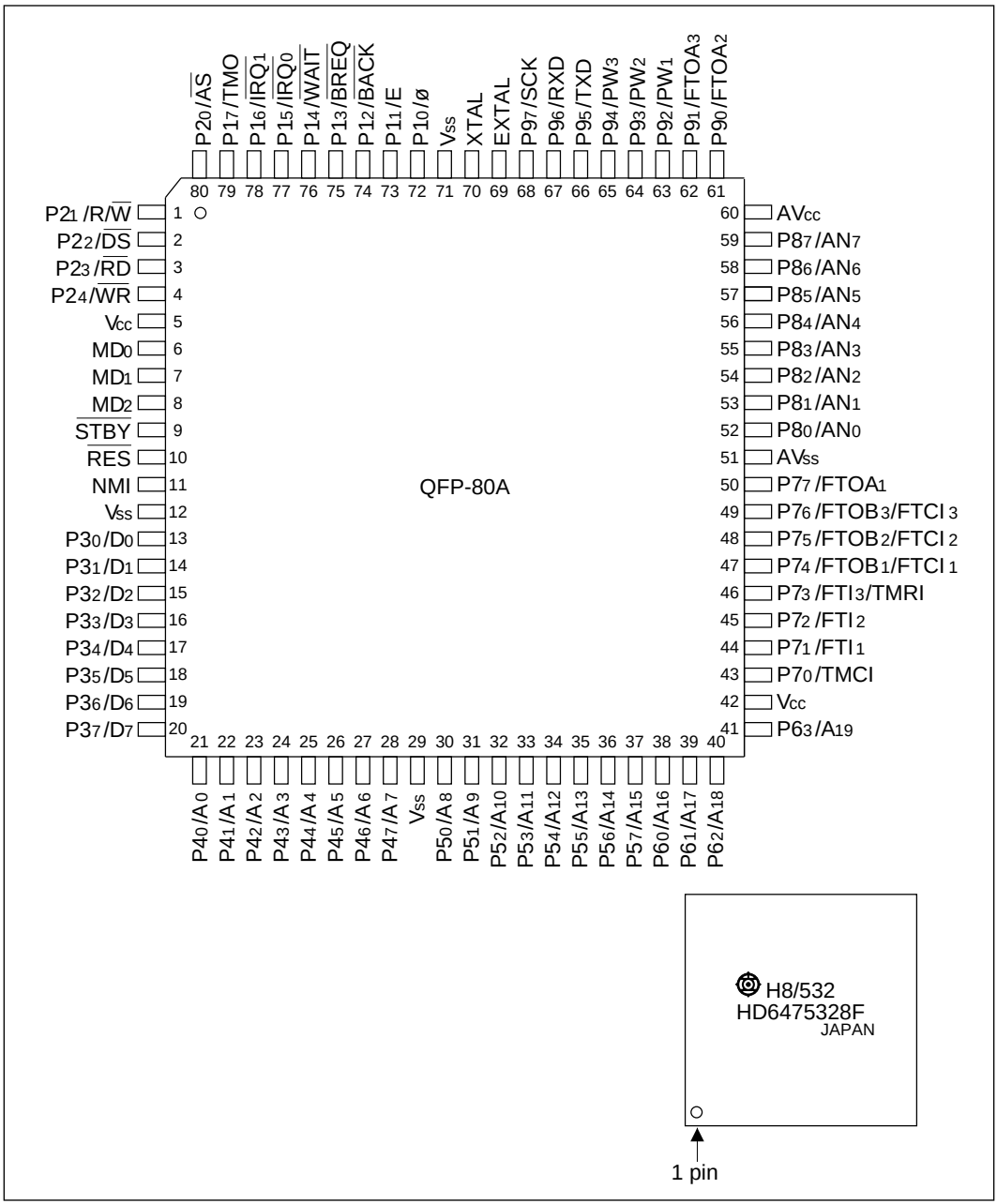

Figure 1-4 Pin Arrangement (FP-80A, Top View)

1.3.2 Pin Functions

Pin Arrangements in Each Operating Mode: Table 1-2 lists the arrangements of the pins of the CP-84 and CG-84 packages in each operating mode. Table 1-3 lists the arrangements for the FP-80A package.

Table 1-2 Pin Arrangements in Each Operating Mode (CP-84, CG-84)

	Pin Name					
	Expanded Minimum Modes		Expanded Maximum Modes		Single-Chip Mode	PROM Mode
Pin No.	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	
1	XTAL	XTAL	XTAL	XTAL	XTAL	NC
2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
3	$P1_0$/ø	$P1_0$/ø	$P1_0$/ø	$P1_0$/ø	$P1_0$/ø	NC
4	$P1_1$/E	$P1_1$/E	$P1_1$/E	$P1_1$/E	$P1_1$/E	NC
5	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$	NC
6	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$	NC
7	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$	NC
8	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	NC
9	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	NC
10	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	NC
11	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$P2_0$	NC
12	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	$P2_1$	NC
13	$\overline{DS}$	$\overline{DS}$	$\overline{DS}$	$\overline{DS}$	$P2_2$	NC
14	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$P2_3$	NC
15	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$P2_4$	NC
16	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
17	MD_0	MD_0	MD_0	MD_0	MD_0	V_{SS}
18	MD_1	MD_1	MD_1	MD_1	MD_1	V_{SS}

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-2 Pin Arrangements in Each Operating Mode (CP-84, CG-84) (cont)

Pin No.	Pin Name					
	Expanded Minimum Modes		Expanded Maximum Modes		Single-Chip Mode	PROM
	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	Mode
19	MD_2	MD_2	MD_2	MD_2	MD_2	V_{SS}
20	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	V_{SS}
21	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	V_{PP}
22	NMI	NMI	NMI	NMI	NMI	A_9
23	NC	NC	NC	NC	NC	NC
24	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
25	D_0	D_0	D_0	D_0	$P3_0$	O_0
26	D_1	D_1	D_1	D_1	$P3_1$	O_1
27	D_2	D_2	D_2	D_2	$P3_2$	O_2
28	D_3	D_3	D_3	D_3	$P3_3$	O_3
29	D_4	D_4	D_4	D_4	$P3_4$	O_4
30	D_5	D_5	D_5	D_5	$P3_5$	O_5
31	D_6	D_6	D_6	D_6	$P3_6$	O_6
32	D_7	D_7	D_7	D_7	$P3_7$	O_7
33	A_0	A_0	A_0	A_0	$P4_0$	A_0
34	A_1	A_1	A_1	A_1	$P4_1$	A_1
35	A_2	A_2	A_2	A_2	$P4_2$	A_2
36	A_3	A_3	A_3	A_3	$P4_3$	A_3
37	A_4	A_4	A_4	A_4	$P4_4$	A_4
38	A_5	A_5	A_5	A_5	$P4_5$	A_5
39	A_6	A_6	A_6	A_6	$P4_6$	A_6
40	A_7	A_7	A_7	A_7	$P4_7$	A_7
41	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-2 Pin Arrangements in Each Operating Mode (CP-84, CG-84) (cont)

Pin No.	Pin Name: Expanded Minimum Modes Mode 1	Expanded Minimum Modes Mode 2	Expanded Maximum Modes Mode 3	Expanded Maximum Modes Mode 4	Single-Chip Mode Mode 7	PROM Mode
42	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
43	A_8	$P5_0$ / A_8	A_8	$P5_0$ / A_8	$P5_0$	A_8
44	A_9	$P5_1$ / A_9	A_9	$P5_1$ / A_9	$P5_1$	OE
45	A_{10}	$P5_2$ / A_{10}	A_{10}	$P5_2$ / A_{10}	$P5_2$	A_{10}
46	A_{11}	$P5_3$ / A_{11}	A_{11}	$P5_3$ / A_{11}	$P5_3$	A_{11}
47	A_{12}	$P5_4$ / A_{12}	A_{12}	$P5_4$ / A_{12}	$P5_4$	A_{12}
48	A_{13}	$P5_5$ / A_{13}	A_{13}	$P5_5$ / A_{13}	$P5_5$	A_{13}
49	A_{14}	$P5_6$ / A_{14}	A_{14}	$P5_6$ / A_{14}	$P5_6$	A_{14}
50	A_{15}	$P5_7$ / A_{15}	A_{15}	$P5_7$ / A_{15}	$P5_7$	CE
51	$P6_0$	$P6_0$	A_{16}	$P6_0$ / A_{16}	$P6_0$	V_{CC}
52	$P6_1$	$P6_1$	A_{17}	$P6_1$ / A_{17}	$P6_1$	V_{CC}
53	$P6_2$	$P6_2$	A_{18}	$P6_2$ / A_{18}	$P6_2$	NC
54	$P6_3$	$P6_3$	A_{19}	$P6_3$ / A_{19}	$P6_3$	NC
55	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
56	$P7_0$ / TMCI	$P7_0$ / TMCI	$P7_0$ / TMCI	$P7_0$ / TMCI	$P7_0$ / TMCI	NC
57	$P7_1$ / FTI_1	$P7_1$ / FTI_1	$P7_1$ / FTI_1	$P7_1$ / FTI_1	$P7_1$ / FTI_1	NC
58	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	NC
59	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	NC
60	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	NC
61	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	NC

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-2 Pin Arrangements in Each Operating Mode (CP-84, CG-84) (cont)

Pin No.	Pin Name: Expanded Minimum Modes Mode 1	Expanded Minimum Modes Mode 2	Expanded Maximum Modes Mode 3	Expanded Maximum Modes Mode 4	Single-Chip Mode Mode 7	PROM Mode
62	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$/ $FTOB_3$ / $FTCI_3$	NC
63	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	NC
64	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
65	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
66	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	NC
67	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	NC
68	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	NC
69	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	NC
70	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	NC
71	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	NC
72	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	NC
73	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	NC
74	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	V_{CC}
75	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	NC
76	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	NC
77	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	NC
78	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	NC
79	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	NC
80	$P9_5$ / TXD	$P9_5$/ TXD	$P9_5$/ TXD	$P9_5$/ TXD	$P9_5$/ TXD	NC
81	$P9_6$ / RXD	$P9_6$/ RXD	$P9_6$/ RXD	$P9_6$/ RXD	$P9_6$/ RXD	NC
82	$P9_7$ / SCK	$P9_7$/ SCK	$P9_7$/ SCK	$P9_7$/ SCK	$P9_7$/ SCK	NC
83	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
84	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	NC

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-3 Pin Arrangements in Each Operating Mode (FP-80A)

Pin	Pin Name					
	Expanded Minimum Modes		Expanded Maximum Modes		Single-Chip Mode	PROM
No.	Mode 1	Mode 2	Mode 3	Mode 4	Mode 7	Mode
1	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	$P2_1$	NC
2	$\overline{DS}$	$\overline{DS}$	$\overline{DS}$	$\overline{DS}$	$P2_2$	NC
3	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$\overline{RD}$	$P2_3$	NC
4	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$\overline{WR}$	$P2_4$	NC
5	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
6	MD_0	MD_0	MD_0	MD_0	MD_0	V_{SS}
7	MD_1	MD_1	MD_1	MD_1	MD_1	V_{SS}
8	MD_2	MD_2	MD_2	MD_2	MD_2	V_{SS}
9	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	$\overline{STBY}$	V_{SS}
10	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	$\overline{RES}$	V_{PP}
11	NMI	NMI	NMI	NMI	NMI	A_9
12	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
13	D_0	D_0	D_0	D_0	$P3_0$	O_0
14	D_1	D_1	D_1	D_1	$P3_1$	O_1
15	D_2	D_2	D_2	D_2	$P3_2$	O_2
16	D_3	D_3	D_3	D_3	$P3_3$	O_3
17	D_4	D_4	D_4	D_4	$P3_4$	O_4
18	D_5	D_5	D_5	D_5	$P3_5$	O_5
19	D_6	D_6	D_6	D_6	$P3_6$	O_6
20	D_7	D_7	D_7	D_7	$P3_7$	O_7
21	A_0	A_0	A_0	A_0	$P4_0$	A_0

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-3 Pin Arrangements in Each Operating Mode (FP-80A) (cont)

Pin No.	Pin Name: Expanded Minimum Modes Mode 1	Expanded Minimum Modes Mode 2	Expanded Maximum Modes Mode 3	Expanded Maximum Modes Mode 4	Single-Chip Mode Mode 7	PROM Mode
22	A_1	A_1	A_1	A_1	$P4_1$	A_1
23	A_2	A_2	A_2	A_2	$P4_2$	A_2
24	A_3	A_3	A_3	A_3	$P4_3$	A_3
25	A_4	A_4	A_4	A_4	$P4_4$	A_4
26	A_5	A_5	A_5	A_5	$P4_5$	A_5
27	A_6	A_6	A_6	A_6	$P4_6$	A_6
28	A_7	A_7	A_7	A_7	$P4_7$	A_7
29	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
30	A_8	$P5_0$ / A_8	A_8	$P5_0$/ A_8	$P5_0$	A_8
31	A_9	$P5_1$ / A_9	A_9	$P5_1$/ A_9	$P5_1$	$\overline{OE}$
32	A_{10}	$P5_2$ / A_{10}	A_{10}	$P5_2$/ A_{10}	$P5_2$	A_{10}
33	A_{11}	$P5_3$ / A_{11}	A_{11}	$P5_3$ / A_{11}	$P5_3$	A_{11}
34	A_{12}	$P5_4$ / A_{12}	A_{12}	$P5_4$ / A_{12}	$P5_4$	A_{12}
35	A_{13}	$P5_5$ / A_{13}	A_{13}	$P5_5$ / A_{13}	$P5_5$	A_{13}
36	A_{14}	$P5_6$ / A_{14}	A_{14}	$P5_6$ / A_{14}	$P5_6$	A_{14}
37	A_{15}	$P5_7$ / A_{15}	A_{15}	$P5_7$ / A_{15}	$P5_7$	$\overline{CE}$
38	$P6_0$	$P6_0$	A_{16}	$P6_0$ / A_{16}	$P6_0$	V_{CC}
39	$P6_1$	$P6_1$	A_{17}	$P6_1$ / A_{17}	$P6_1$	V_{CC}
40	$P6_2$	$P6_2$	A_{18}	$P6_2$ / A_{18}	$P6_2$	NC
41	$P6_3$	$P6_3$	A_{19}	$P6_3$ / A_{19}	$P6_3$	NC
42	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-3 Pin Arrangements in Each Operating Mode (FP-80A) (cont)

Pin No.	Pin Name: Expanded Minimum Modes Mode 1	Expanded Minimum Modes Mode 2	Expanded Maximum Modes Mode 3	Expanded Maximum Modes Mode 4	Single-Chip Mode Mode 7	PROM Mode
43	$P7_0$ / TMCI	$P7_0$/ TMCI	$P7_0$/ TMCI	$P7_0$/ TMCI	$P7_0$/ TMCI	NC
44	$P7_1$ / FTI_1	$P7_1$/ FTI_1	$P7_1$/ FTI_1	$P7_1$/ FTI_1	$P7_1$/ FTI_1	NC
45	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	$P7_2$ / FTI_2	NC
46	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	$P7_3$ / FTI_3 / TMRI	NC
47	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	$P7_4$/ $FTOB_1$ / $FTCI_1$	$P7_4$ / $FTOB_1$ / $FTCI_1$	NC
48	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	$P7_5$ / $FTOB_2$ / $FTCI_2$	NC
49	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	$P7_6$ / $FTOB_3$ / $FTCI_3$	NC
50	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	$P7_7$ / $FTOA_1$	NC
51	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	AV_{SS}	V_{SS}
52	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	$P8_0$ / AN_0	NC
53	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	$P8_1$ / AN_1	NC
54	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	$P8_2$ / AN_2	NC
55	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	$P8_3$ / AN_3	NC
56	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	$P8_4$ / AN_4	NC
57	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	$P8_5$ / AN_5	NC
58	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	$P8_6$ / AN_6	NC
59	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	$P8_7$ / AN_7	NC

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Table 1-3 Pin Arrangements in Each Operating Mode (FP-80A) (cont)

Pin No.	Pin Name: Expanded Minimum Modes Mode 1	Expanded Minimum Modes Mode 2	Expanded Maximum Modes Mode 3	Expanded Maximum Modes Mode 4	Single-Chip Mode Mode 7	PROM Mode
60	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	V_{CC}
61	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	$P9_0$ / $FTOA_2$	NC
62	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	$P9_1$ / $FTOA_3$	NC
63	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	$P9_2$ / PW_1	NC
64	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	$P9_3$ / PW_2	NC
65	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	$P9_4$ / PW_3	NC
66	$P9_5$ / TXD	$P9_5$ / TXD	$P9_5$ / TXD	$P9_5$ / TXD	$P9_5$ / TXD	NC
67	$P9_6$ / RXD	$P9_6$ / RXD	$P9_6$ / RXD	$P9_6$ / RXD	$P9_6$ / RXD	NC
68	$P9_7$ / SCK	$P9_7$ / SCK	$P9_7$ / SCK	$P9_7$ / SCK	$P9_7$ / SCK	NC
69	EXTAL	EXTAL	EXTAL	EXTAL	EXTAL	NC
70	XTAL	XTAL	XTAL	XTAL	XTAL	NC
71	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
72	$P1_0$ / ø	$P1_0$ / ø	$P1_0$ / ø	$P1_0$ / ø	$P1_0$ / ø	NC
73	$P1_1$ / E	$P1_1$ / E	$P1_1$ / E	$P1_1$ / E	$P1_1$ / E	NC
74	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$ / $\overline{BACK}$	$P1_2$	NC
75	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$ / $\overline{BREQ}$	$P1_3$	NC
76	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$ / $\overline{WAIT}$	$P1_4$	NC
77	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	$P1_5$ / $\overline{IRQ_0}$	NC
78	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	$P1_6$ / $\overline{IRQ_1}$	NC
79	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	$P1_7$ / TMO	NC
80	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$\overline{AS}$	$P2_0$	NC

Notes: 1. For the PROM mode, see section 17, “ROM.”
2. Pins marked NC should be left unconnected.

Pin Functions: Table 1-4 gives a concise description of the function of each pin.

Table 1-4 Pin Functions

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
Power	V_{CC}	16, 55	5, 42	I	**Power:** Connected to the power supply (+5V). Connect both V_{CC} pins to the system power supply (+5V). The chip will not operate if either pin is left unconnected.
	V_{SS}	2, 24 41, 42 64, 83	12, 29 71	I	**Ground:** Connected to ground (0V). Connect all V_{SS} pins to the system power supply (0V). The chip will not operate if any V_{SS} pin is left unconnected.
Clock	XTAL	1	70	I	**Crystal:** Connected to a crystal oscillator. The crystal frequency should be double the desired ø clock frequency. If an external clock is input at the EXTAL pin, leave the XTAL pin unconnected.
	EXTAL	84	69	I	**External Crystal:** Connected to a crystal oscillator or external clock. The frequency of the external clock should be double the desired ø clock frequency. See section 8.2, “Oscillator Circuit” for examples of connections to a crystal and external clock.
	ø	3	72	O	**System Clock:** Supplies the ø clock to peripheral devices.
	E	4	73	O	**Enable Clock:** Supplies an E clock to E clock based peripheral devices.
System control	$\overline{\text{BACK}}$	5	74	O	**Bus Request Acknowledge:** Indicates that the bus right has been granted to an external device. Notifies an external device that issued a $\overline{\text{BREQ}}$ signal that it now has control of the bus.

Table 1-4 Pin Functions (cont)

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
System control	$\overline{\text{BREQ}}$	6	75	I	**Bus Request:** Sent by an external device to the H8/532 chip to request the bus right.
	$\overline{\text{STBY}}$	20	9	I	**Standby:** A transition to the hardware standby mode (a power-down state) occurs when a Low input is received at the $\overline{\text{STBY}}$ pin.
	$\overline{\text{RES}}$	21	10	I	**Reset:** A Low input causes the H8/532 chip to reset.
Address bus	$A_{19} – A_0$	54 – 43 40 – 33	41 – 30 28 – 21	O	**Address Bus:** Address output pins.
Data bus	$D_7 – D_0$	32 – 25	20 – 13	I/O	**Data Bus:** 8-Bit bidirectional data bus.
Bus control	$\overline{\text{WAIT}}$	7	76	I	**Wait:** Requests the CPU to insert one or more Tw states when accessing an off-chip address.
	$\overline{\text{AS}}$	11	80	O	**Address Strobe:** Goes Low to indicate that there is a valid address on the address bus.
	R/$\overline{\text{W}}$	12	1	O	**Read/Write:** Indicates whether the CPU is reading or writing data on the bus. • High—Read • Low—Write
	$\overline{\text{DS}}$	13	2	O	**Data Strobe:** Goes Low to indicate the presence of valid data on the data bus.
	$\overline{\text{RD}}$	14	3	O	**Read:** Goes Low to indicate that the CPU is reading an external address.
	$\overline{\text{WR}}$	15	4	O	**Write:** Goes Low to indicate that the CPU is writing to an external address.

Table 1-4 Pin Functions (cont)

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
Interrupt	NMI	22	11	I	**NonMaskable Interrupt:** Highest-signals priority interrupt request. The port 1 control register (P1CR) determines whether the interrupt is requested on the rising or falling edge of the NMI input.
	$\overline{IRQ_0}$	8	77	I	**Interrupt Request 0 and 1:** Maskable interrupt request pins.
	$\overline{IRQ_1}$	9	78		
Operating mode control	MD_2	19	8	I	**Mode:** Input pins for setting the MCU operating mode according to the table below.
	MD_1	18	7		
	MD_0	17	6		

MD_2	MD_1	MD_0	Mode	Description
0	0	0	Mode 0	—
0	0	1	Mode 1	Expanded minimum mode (ROM disabled)
0	1	0	Mode 2	Expanded minimum mode (ROM enabled)
0	1	1	Mode 3	Expanded maximum mode (ROM disabled)
1	0	0	Mode 4	Expanded maximum mode (ROM enabled)
1	0	1	Mode 5	—
1	1	0	Mode 6	—
1	1	1	Mode 7	Single-chip mode

The inputs at these pins are latched in mode select bits 2 to 0 (MDS2 – MDS0) of the mode control register (MDCR) on the rising edge of the $\overline{RES}$ signal.

Table 1-4 Pin Functions (cont)

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
16-Bit free-running timer (FRT)	FTOA1	63	50	O	**FRT Output Compare A (channels 1, 2, and 3):** Output pins for the output compare A function of the free-running timer channels 1, 2, and 3.
	FTOA2	75	61		
	FTOA3	76	62		
	FTOB1	60	47	O	**FRT Output Compare B (channels 1, 2, and 3):** Output pins for the output compare B function of the free-running timer channels 1, 2, and 3.
	FTOB2	61	48		
	FTOB3	62	49		
	FTCI1	60	47	I	**FRT Counter Clock Input (channels 1, 2, and 3):** External clock input pins for the free-running counters (FRCs) of free-running timer channels 1, 2, and 3.
	FTCI2	61	48		
	FTCI3	62	49		
	FTI1	57	44	I	**FRT Input Capture (channels 1, 2, and 3):** Input capture pins for free-running timer channels 1, 2, and 3.
	FTI2	58	45		
	FTI3	59	46		
8-Bit timer	TMO	10	79	O	**8-bit Timer Output:** Compare-match output pin for the 8-bit timer.
	TMCI	56	43	I	**8-bit Timer Clock Input:** External clock input pin for the 8-bit timer counter.
	TMRI	59	46	I	**8-bit Timer Counter Reset Input:** A high input at this pin resets the 8-bit timer counter.
PWM timer	PW1	77	63	O	**PWM Timer Output (channels 1, 2, and 3):** Pulse-width modulation timer output pulses.
	PW2	78	64		
	PW3	79	65		

Table 1-4 Pin Functions (cont)

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
Serial communication interface signals	TXD	80	66	O	**Transmit Data:** Data output pins for the serial communication interface.
	RXD	81	67	I	**Receive Data:** Data input pins for the serial communication interface.
	SCK	82	68	I/O	**Serial Clock:** Input/output pin for the serial interface clock.
A/D converter	AN_7 – AN_0	73 – 66	59 – 52	I	**Analog Input:** Analog signal input pins.
	AV_{CC}*	74	60	I	**Analog Reference Voltage:** Reference voltage and power supply pin for the A/D converter.
	AV_{SS}*	65	51	I	**Analog Ground:** Ground pin for the A/D converter.
Parallel I/O	$P1_7$ – $P1_0$	10 – 3	79 – 72	I/O	**Port 1:** An 8-bit input/output port. The direction of each bit is determined by the port 1 data direction register (P1DDR).
	$P2_4$ – $P2_0$	15 – 11	4 – 1, 80	I/O	**Port 2:** A 5-bit input/output port. The direction of each bit is determined by the port 2 data direction register (P2DDR).
	$P3_7$ – $P3_0$	32 – 25	20 – 13	I/O	**Port 3:** An 8-bit input/output port. The direction of each bit is determined by the port 3 data direction register (P3DDR).
	$P4_7$ – $P4_0$	40 – 33	28 – 21	I/O	**Port 4:** An 8-bit input/output port. The direction of each bit is determined by the port 4 data direction register (P4DDR). These pins can drive LED indicators.

* When A/D converter is not used, AV_{CC} should be connected to V_{CC}, and AV_{SS} should be connected to GND.

Table 1-4 Pin Functions (cont)

Type	Symbol	Pin No. CP-84, CG-84	Pin No. FP-80A	I/O	Name and Function
Parallel I/O	$P5_7$ – $P5_0$	50 – 43	37 – 30	I/O	**Port 5:** An 8-bit input/output port. The direction of each bit is determined by the port 5 data direction register (P5DDR). These pins have built-in MOS input pull-ups.
	$P6_3$ – $P6_0$	54 – 51	41 – 38	I/O	**Port 6:** A 4-bit input/output port. The direction of each bit is determined by the port 6 data direction register (P6DDR). These pins have built-in MOS input pull-ups.
	$P7_7$ – $P7_0$	63 – 56	50 – 43	I/O	**Port 7:** An 8-bit input/output port. The direction of each bit is determined by the port 7 data direction register (P7DDR). These pins have Schmitt inputs.
	$P8_7$ – $P8_0$	73 – 66	59 – 52	I	**Port 8:** An 8-bit input port
	$P9_7$ – $P9_0$	82 – 75	68 – 61	I/O	**Port 9:** An 8-bit input/output port. The direction of each bit is determined by the port 9 data direction register (P9DDR).