Section 2 MCU Operating Modes and Address Space

2.1 Overview

The H8/532 microcomputer unit (MCU) operates in five modes numbered 1, 2, 3, 4, and 7. The mode is selected by the inputs at the mode pins (MD_2 to MD_0) at the instant when the chip comes out of a reset. As indicated in table 2-1, the MCU mode determines the size of the address space, the usage of on-chip ROM, and the operating mode of the CPU. The MCU mode also affects the functions of I/O pins.

Table 2-1 Operating Modes

MD_2	MD_1	MD_0	MCU Mode	Address Space	On-Chip ROM	CPU Mode
0	0	0	—	—	—	—
0	0	1	Mode 1	Expanded minimum	Disabled	Minimum mode
0	1	0	Mode 2	Expanded minimum	Enabled	Minimum mode
0	1	1	Mode 3	Expanded maximum	Disabled	Maximum mode
1	0	0	Mode 4	Expanded maximum	Enabled	Maximum mode
1	0	1	—	—	—	—
1	1	0	—	—	—	—
1	1	1	Mode 7	Single-chip only	Enabled	Minimum mode

Notation: 0: Low level
1: High level
—: Cannot be used

Modes 1 to 4 are referred to as “expanded” because they permit access to off-chip memory and peripheral addresses. The expanded minimum modes (modes 1 and 2) support a maximum address space of 64K bytes. The expanded maximum modes (modes 3 and 4) support a maximum address space of 1M byte.

Interrupt service is slightly slower in the expanded maximum modes than in the other modes because the CPU has to save its code page register.

The H8/532 cannot be set to modes 0, 5, and 6. The mode pins should never be set to these values.

2.2 Mode Descriptions

The five MCU modes are described below. For further information on the I/O pin functions in each mode, see section 9, “I/O Ports.”

Mode 1 (Expanded Minimum Mode): Mode 1 supports a maximum 64K-byte address space which does not include any on-chip ROM. Ports 1 to 5 are used for bus lines and bus control signals as follows:

Control signals: Ports 1* and 2
Data bus: Port 3
Address bus: Ports 4 and 5

* The functions of individual pins of port 1 are software-selectable.

Mode 2 (Expanded Minimum Mode): Mode 2 supports a maximum 64K-byte address space of which the first 32K bytes are in on-chip ROM. Ports 1 to 5 are used for bus lines and bus control signals as follows:

Control signals: Ports 1* and 2
Data bus: Port 3
Address bus: Ports 4 and 5*

* The functions of individual pins in ports 1 and 5 are software-selectable.

Note: In mode 2, port 5 is initially a general-purpose input port. Software must change it to output before using it for the address bus. See section 9.6, “Port 5” for details. The following instruction makes all pins of port 5 into output pins:

```
MOV.B  #H'FF, @H'FF88*
```

* H'xx or H'xxxx express the hexadecimal number.

Mode 3 (Expanded Maximum Mode): Mode 3 supports a maximum 1M-byte address space which does not include any on-chip ROM. Ports 1 to 6 are used for bus lines and bus control signals as follows:

Control signals: Ports 1* and 2
Data bus: Port 3
Address bus: Ports 4, 5, and 6

* The functions of individual pins of port 1 are software-selectable.

Mode 4 (Expanded Maximum Mode): Mode 4 supports a maximum 1M-byte address space of which the first 32K bytes are in on-chip ROM. Ports 1 to 6 are used for bus lines and bus control signals as follows:

Control signals: Ports 1* and 2
Data bus: Port 3
Address bus: Ports 4, 5*, and 6*

* The functions of individual pins in ports 1, 5, and 6 are software-selectable.

Note: In mode 4, ports 5 and 6 are initially general-purpose input ports. Software must change them to output before using them for the address bus. See section 9.6, “Port 5” and 10.7, “Port 6” for details. The following instruction sets all pins of ports 5 and 6 to output:

```
MOV.W #H'FFFF, @H'FF88
```

Mode 7 (Single-Chip Mode): In this mode all memory is on-chip, in 32K bytes of ROM and 1K byte of RAM. It is not possible to access off-chip addresses.

The single-chip mode provides the maximum number of ports. All the pins associated with the address and data buses in the expanded modes are available as general-purpose input/output ports in the single-chip mode.

2.3 Address Space Map

2.3.1 Page Segmentation

The H8/532’s address space is segmented into 64K-byte pages. In the single-chip mode and expanded minimum modes there is just one page: page 0. In the expanded maximum modes there can be up to 16 pages. Figure 2-1 shows the address space in each mode and indicates which parts are on- and off-chip.

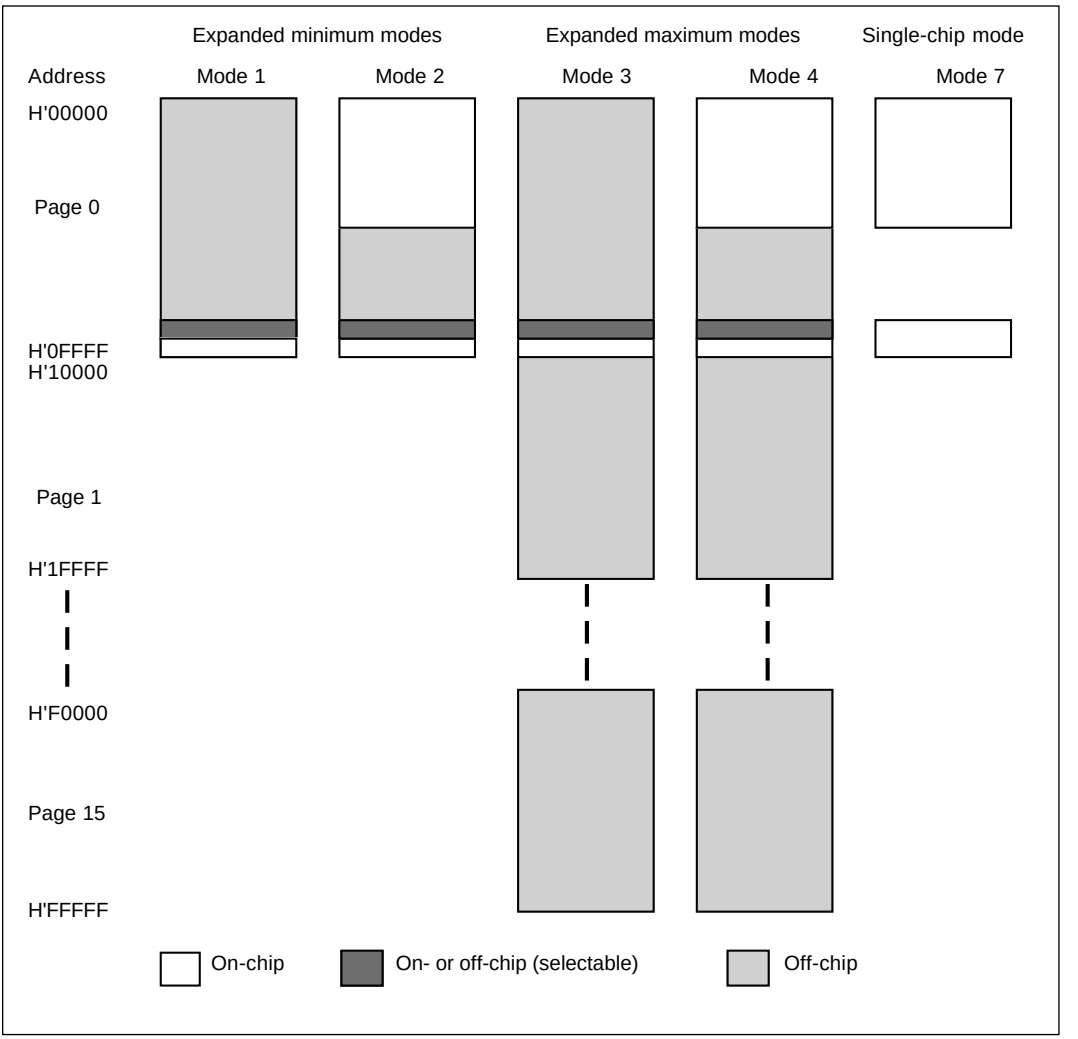

Figure 2-1 Address Space in Each Mode

2.3.2 Page 0 Address Allocations

The high and low address areas in page 0 are reserved for registers and vector tables.

Vector Tables: The low address area contains the exception vector table and DTC vector table. The CPU accesses the exception vector table to obtain the addresses of user-coded exception-handling routines. The DTC vector table contains pointers to tables of register information used by the on-chip chip data transfer controller. The size of these tables depends on the CPU operating mode. Details are given in section 4.1.3, “Exception Factors and Vector Table,” section 5.2.3, “Interrupt Vector Table,” and section 6.3.2, “DTC Vector Table.”

In modes 2 and 4 the vector tables are located in on-chip ROM. In modes 1, 3, and 7 the vector tables are in external memory.

Register Field: The highest 128 addresses in page 0 (addresses H'FF80 to H'FFFF) belong to control, status, and data registers used by the I/O ports and on-chip supporting modules. Program code cannot be located at these addresses.

The CPU accesses addresses in this register field like other addresses in the address space. By reading and writing at these addresses the CPU controls the on-chip supporting modules and communicates via the I/O ports. A complete map of the register field is given in appendix B.

On-Chip RAM: One of the control registers in the register field is a RAM control register (RAMCR) containing a RAM enable bit (RAME) that enables or disables the 1-kbyte on-chip RAM. When this bit is set to “1” (its default value), addresses H'FFB0 to H'FF7F are located on-chip. When this bit is cleared to “0,” these addresses are located in external memory and the on-chip RAM is not used. See section 16, “RAM” for further information.

The RAME bit is bit 7 at address H'FFF9.

Coding Example:
To enable on-chip RAM: `BSET.B #7, @H'FFF9`
To disable on-chip RAM: `BCLR.B #7, @H'FFF9`

Note: If on-chip RAM is disabled in the single-chip mode, access to addresses H'FFB0 to H'FF7F causes an address error.

Figure 2-2 is a map of page 0 of the address space.

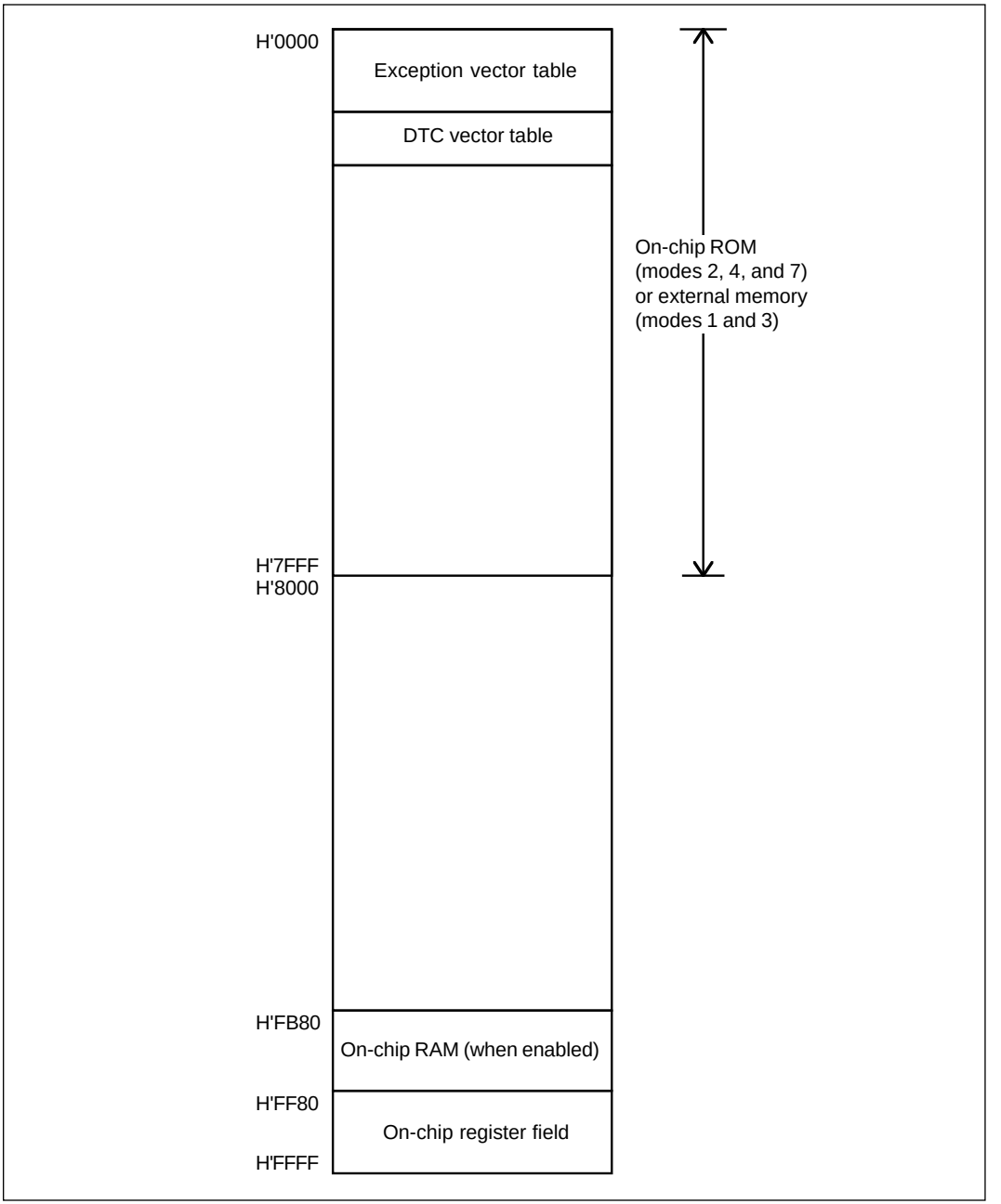

Figure 2-2 Map of Page 0

2.4 Mode Control Register (MDCR)

Another control register in the register field in page 0 is the mode control register (MDCR). The inputs at the mode pins are latched in this register on the rising edge of the signal. The mode control register can be read by the CPU, but not written. Table 3-2 lists the attributes of this register.

Table 2-2 Mode Control Register

Name	Abbreviation	Read/Write	Address
Mode control register	MDCR	Read only	H'FFFA

The bit configuration of this register is shown below.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	MDS2	MDS1	MDS0
Initial value	1	1	0	0	0	*	*	*
Read/Write	—	—	—	—	—	R	R	R

* Initialized according to MD_2 to MD_0.

Bits 7 and 6—Reserved: These bits cannot be modified and are always read as “1.”

Bits 5 to 3—Reserved: These bits cannot be modified and are always read as “0.”

Bits 2 to 0—Mode Select 2 to 0 (MDS2 to MDS0): These bits indicate the values of the mode pins (MD_2 to MD_0) latched on the rising edge of the signal. MDS2 corresponds to MD_2, MDS1 to MD_1, and MDS0 to MD_0. These bits can be read but not written.

Coding Example: To test whether the MCU is operating in mode 1:

```
CMP:G.B #H'C1, @H'FFFA
```

The comparison is with H'C1 instead of H'01 because bits 7 and 6 are always read as “1.”