Section 9 I/O Ports

9.1 Overview

The H8/532 has nine ports. Ports 1, 3, 4, 5, 7, and 9 are eight-bit input/output ports. Port 2 is a five-bit input/output port. Port 6 is a four-bit input/output port. Port 8 is an eight-bit input-only port. Table 9-1 summarizes the functions of each port.

Input and output are memory-mapped. The CPU views each port as a data register (DR) located in the register field at the high end of page 0 of the address space. Each port (except port 8) also has a data direction register (DDR) which determines which pins are used for input and which for output. Port 1 has an additional control register (P1CR) for enabling and disabling IRQ_0 and IRQ_1 and setting other controls.

To read data from an I/O port, the CPU selects input in the data direction register and reads the data register. This causes the input logic level at the pin to be placed directly on the internal data bus. There is no intervening input latch.

To send data to an output port, the CPU selects output in the data direction register and writes the desired data in the data register, causing the data to be held in a latch. The latch output drives the pin through a buffer amplifier. If the CPU reads the data register of an output port, it obtains the data held in the latch rather than the actual level of the pin.

As table 9-1 indicates, all of the I/O port pins have dual functions. For example, pin 7 of port 1 can be used either as a general-purpose I/O pin ($P1_7$), or for output of the TMO signal from the on-chip 8-bit timer. The function is determined by the MCU operating mode, or by a value set in a control register.

Outputs from ports 1 to 6 can drive one TTL load and a 90pF capacitive load. Outputs from ports 7 and 9 can drive one TTL load and a 30pF capacitive load.

Outputs from ports 1 to 7 and 9 can also drive a Darlington transistor pair. Outputs from port 4 can drive a light-emitting diode (with 10mA current sink). Ports 5 and 6 have built-in MOS pull-ups for each input. Port 7 has Schmitt inputs.

Schematic diagrams of the I/O port circuits are shown in appendix C.

Table 9-1 Input/Output Port Summary

Port	Description	Pins	Expanded Modes				Single-Chip Mode (Mode 7)
			Mode 1	Mode 2	Mode 3	Mode 4	
Port 1	8-Bit input/output	$P1_7$ / TMO $P1_6$ / $\overline{IRQ_1}$ $P1_5$ / $\overline{IRQ_0}$	These input/output pins double as and inputs and as $\overline{IRQ_0}$ and $\overline{IRQ_1}$ input and output pin (TMO) for the 8-bit timer.				
		$P1_4$ / $\overline{WAIT}$ $P1_3$ / $\overline{BREQ}$ $P1_2$ / $\overline{BACK}$	These pins function as $\overline{WAIT}$, $\overline{BREQ}$, and $\overline{BACK}$ when necessary control-register bits are set to “1.”				Input/output port
		$P1_1$ / E $P1_0$ / ø	These pins function as input pins or as clock (E, ø) output pins, depending on the data direction register setting.				
Port 2	5-Bit input/output port	$P2_4$ / $\overline{WR}$ $P2_3$ / $\overline{RD}$ $P2_2$ / $\overline{DS}$ $P2_1$ / R/$\overline{W}$ $P2_0$ / $\overline{AS}$	Bus control signal outputs ($\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$)				Input/output port
Port 3	8-Bit input/output port	$P3_7$ - $P3_0$ / D_7 – D_0	Data bus (D_7 – D_0)				Input/output port
Port 4	8-Bit input/output port Can drive a LED	$P4_7$ – $P4_0$ / A_7 – A_0	Low address bits (A_7 – A_0)				Input/output port
Port 5	8-Bit input/output port Built-in input pull-up (MOS)	$P5_7$ – $P5_0$ / A_{15} – A_8	High address bus (A_{15} – A_8)	High address bus if DDR is set to “1”	High address bus (A_{15} – A_8)	High address bus if DDR is set to “1”	Input/output port
Port 6	4-Bit input/output port Built-in input pull-up (MOS)	$P6_3$ –$P6_0$ / A_{19} – A_{16}	Input/output port		Page address bus (A_{19} – A_{16})	Page address bus if DDR is set to “1,” input port if DDR is set to “0”	Input/output port

Table 9-1 Input/Output Port Summary (cont)

Port	Description	Pins	Expanded Modes Mode 1 Mode 2 Mode 3 Mode 4	Single-Chip Mode (Mode 7)
Port 7	8-Bit input/output port (Schmitt inputs)	$P7_7$ / $FTOA_1$ $P7_6$ / $FTOB_3$ / $FTCI_3$ $P7_5$ / $FTOB_2$ / $FTCI_2$ $P7_4$ / $FTOB_1$ / $FTCI_1$ / $P7_3$ / FTI_3 TMRI $P7_2$ / FTI_2 $P7_1$ / FTI_1 $P7_0$ / TMCI	Input/output for free-running timers 1, 2 and 3 (FTI_1 to FTI_3, $FTCI_1$ to $FTCI_3$, $FTOB_1$ to $FTOB_3$, $FTOA_1$),input for 8-bit timer input (TMCI, TMRI), and 8-bit input/output port ($P7_7$ to $P7_0$)	
Port 8	8-Bit input port	$P8_0$ - $P8_7$ AN_7 – AN_0	Analog input pins for A/D converter, and 8-bit input port	
Port 9	8-Bit input/output port	$P9_7$ / SCK $P9_6$ / RXD $P9_5$ / TXD $P9_4$ / PW_3 $P9_3$ / PW_2 $P9_2$ / PW_1 $P9_1$ / $FTOA_3$ $P9_0$ / $FTOA_2$	Output for free-running timers 2 and 3 ($FTOA_2$, $FTOA_3$), PWM timer output (PW_1, PW_2, PW_3), serial communication interface (SCI) input/output (TXD, RXD, SCK), and 8-bit input/output port	

9.2 Port 1

9.2.1 Overview

Port 1 is an 8-bit input/output port with the pin configuration shown in figure 9-1. All pins have dual functions, except that in the single-chip mode pins 4, 3, and 2 do not have the WAIT, BREQ, and BACK functions. (because the CPU does not access an external bus.)

Outputs from port 1 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair.

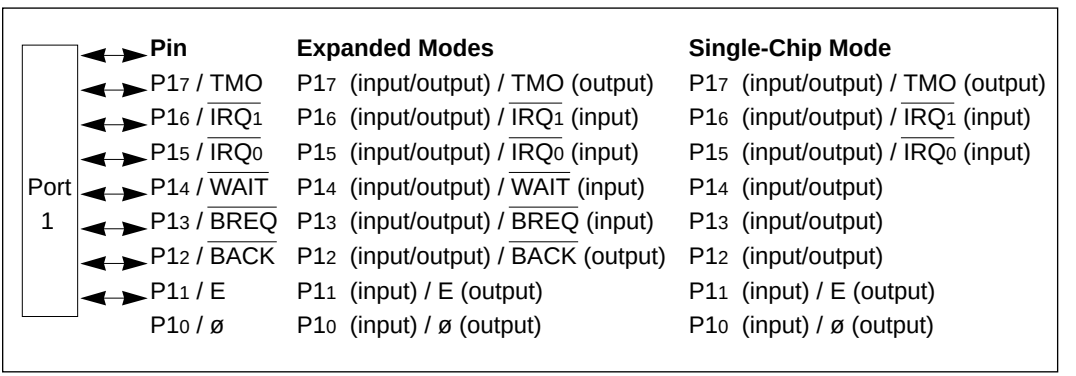

Figure 9-1 Pin Functions of Port 1

9.2.2 Port 1 Registers

Register Configuration: Table 9-2 lists the registers of port 1.

Table 9-2 Port 1 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 1 data direction register	P1DDR	W	H'03	H'FF80
Port 1 data register	P1DR	R/W*1	Undetermined*2	H'FF82
Port 1 control register	P1CR	R/W	H'87	H'FFFC

*1 Bits 1 and 0 are read-only.

*2 Bits 1 and 0 are undetermined. Other bits are initialized to “0.”

1. Port 1 Data Direction Register (P1DDR)—H'FF80

Bit	7	6	5	4	3	2	1	0
	$P1_7$DDR	$P1_6$DDR	$P1_5$DDR	$P1_4$DDR	$P1_3$DDR	$P1_2$DDR	$P1_1$DDR	$P1_0$DDR
Initial value	0	0	0	0	0	0	1	1
Read/Write	W	W	W	W	W	W	W	W

P1DDR is an 8-bit register that selects the direction of each pin in port 1. A pin functions as an output pin if the corresponding bit in P1DDR is set to "1," and as an input pin if the bit is cleared to "0."

P1DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as "1," regardless of their true values.

A reset initializes P1DDR to H'03, so that pins $P1_1$ and $P1_0$ carry clock outputs and the other pins are set for input. In the hardware standby mode, P1DDR is cleared to H'00, stopping the clock outputs. P1DDR is not initialized in the software standby mode, so if a P1DDR bit is set to "1" when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 1 data register (or the ø or E clock).

2. Port 1 Data Register (P1DR)—H'FF82

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R

P1DR is an 8-bit register containing the data for pins $P1_7$ to $P1_0$. When the CPU reads P1DR, for output pins it reads the value in the P1DR latch, but for input pins, it obtains the pin status directly.
Note that when pins $P1_1$ and $P1_0$ are used for output, they output the clock signals (ø and E), not the contents of P1DR. If the CPU reads Pl_1 and Pl_0 (when Pl_1DDR = Pl_0DDR = 1), it obtains the clock values at the current instant.

3. Port 1 Control Register (P1CR)—H'FFFC

Bit	7	6	5	4	3	2	1	0
	—	IRQ_1E	IRQ_0E	NMIEG	BRLE	—	—	—
Initial value	1	0	0	0	0	1	1	1
Read/Write	—	R/W	R/W	R/W	R/W	—	—	—

P1CR selects the functions of four of the port 1 pins. It also selects the input edge of the NMI pin.

At a reset and in the hardware standby mode, P1CR is initialized to H'87. It is not initialized in the software standby mode.

Bit 7—Reserved: This bit cannot be modified and is always read as "1."

Bit 6—Interrupt Request 1 Enable (IRQ1E): This bit selects the function of pin P16.

Bit 6

IRQ1E	Description	
0	P16 functions as an input/output pin.	(Initial value)
1	P16 functions as the $\overline{\text{IRQ}}_1$ input pin, regardless of the value set in P16DDR. (However, the CPU can still read the pin status by reading P1DR.)	

Bit 5—Interrupt Request 0 Enable (IRQ0E): This bit selects the function of pin P15.

Bit 5

IRQ0E	Description	
0	P15 functions as an input/output pin.	(Initial value)
1	P15 functions as the $\overline{\text{IRQ}}_0$ input pin, regardless of the value set in P15DDR. (However, the CPU can still read the pin status by reading P1DR.)	

Bit 4—Nonmaskable Interrupt Edge (NMIEG): This bit selects the input edge of the NMI pin. It is not related to port 0.

Bit 4

NMIEG	Description	
0	A nonmaskable interrupt is generated on the falling edge of the input at the NMI pin.	(Initial value)
1	A nonmaskable interrupt is generated on the rising edge of the input at the NMI pin.	

Bit 3—Bus Release Enable (BRLE): This bit selects the functions of pins P12 and P13. It is valid only in the expanded modes (modes 1, 2, 3, and 4). In the single-chip mode, pins P12 and P13 function as input/output pins regardless of the value of the BRLE bit.

Bit 3 BRLE	Description	
0	$P1_3$ and $P1_2$ function as input/output pins.	(Initial value)
1	$P1_3$ functions as the input pin. $P1_2$ functions as the output pin.	

Bits 2 to 0—Reserved: These bits cannot be modified and are always read as “1.”

9.2.3 Pin Functions in Each Mode

Port 1 operates differently in the expanded modes (modes 1, 2, 3, and 4) and the single-chip mode (mode 7). Table 9-3 explains how the pin functions are selected in the expanded mode. Table 9-4 explains how the pin functions are selected in the single-chip mode.

Table 9-3 Port 1 Pin Functions in Expanded Modes

Pin	Functions and How they are Selected
$P1_7$ / TMO	The function depends on output select bits 3 to 0 (OS3 to OS0) of the 8-bit timer control/status register (TCSR) and on the $P1_7$DDR bit as follows:

OS3 to OS0	All four bits are “0”		At least one bit is “1”	
$P1_7$DDR	0	1	0	1
Pin function	$P1_7$ input	$P1_7$ output	TMO output	

$P1_6$ / $\overline{IRQ_1}$	The function depends on the IRQ_1E bit and the $P1_6$DDR bit as follows:

IRQ_1E	0		1	
$P1_6$DDR	0	1	0	1
Pin function	$P1_6$ input	$P1_6$ output	$\overline{IRQ_1}$ input	

$P1_5$ / $\overline{IRQ_0}$	The function depends on the IRQ_0E bit and the $P1_5$DDR bit as follows:

IRQ_0E	0		1	
$P1_5$DDR	0	1	0	1
Pin function	$P1_5$ input	$P1_5$ output	$\overline{IRQ_0}$ input	

Table 9-3 Port 1 Pin Functions in Expanded Modes (cont)

Pin	Functions and How they are Selected

P1$_4$ / $\overline{\text{WAIT}}$ The function depends on the wait mode select 1 bit (WMS1) of the wait-state control register (WCR) and the P1$_4$DDR bit as follows:

WMS1	0		1	
P1$_4$DDR	0	1	0	1
Pin function	P1$_4$ input	P1$_4$ output	$\overline{\text{WAIT}}$ input	

P1$_3$ / $\overline{\text{BREQ}}$ The function depends on the BRLE bit and the P1$_3$DDR bit as follows:

BRLE	0		1	
P1$_3$DDR	0	1	0	1
Pin function	P1$_3$ input	P1$_3$ output	$\overline{\text{BREQ}}$ input	

P1$_2$ / $\overline{\text{BACK}}$ The function depends on the BRLE bit and the P1$_2$DDR bit as follows:

BRLE	0		1	
P1$_2$DDR	0	1	0	1
Pin function	P1$_2$ input	P1$_2$ output	$\overline{\text{BACK}}$ input	

P1$_1$ / E

P1$_1$DDR	0	1
Pin function	Input	E clock output

P1$_0$ / ø

P1$_0$DDR	0	1
Pin function	Input	ø clock output

Table 9-4 Port 1 Pin Functions in Single-Chip Modes

Pin	Selection of Pin Functions
$P1_7$ / TMO	The function depends on output select bits 3 to 0 (OS3 to OS0) of the 8-bit timer control/status register (TCSR) and on the $P1_7$DDR bit as follows:

OS3 to OS0	All four bits are “0”		At least one bit is “1”	
$P1_7$DDR	0	1	0	1
Pin function	$P1_7$ input	$P1_7$ output	TMO output	

$P1_6$ / $\overline{IRQ_1}$	The function depends on the IRQ_1E bit and the $P1_6$DDR bit as follows:

IRQ_1E	0		1	
$P1_6$DDR	0	1	0	1
Pin function	$P1_6$ input	$P1_6$ output	$\overline{IRQ_1}$ input	

$P1_5$ / $\overline{IRQ_0}$	The function depends on the IRQ_0E bit and the $P1_5$DDR bit as follows:

IRQ_0E	0		1	
$P1_5$DDR	0	1	0	1
Pin function	$P1_5$ input	$P1_5$ output	$\overline{IRQ_0}$ input	

$P1_4$

$P1_4$DDR	0	1
Pin function	Input	Output

$P1_3$

$P1_3$DDR	0	1
Pin function	Input	Output

Table 9-4 Port 1 Pin Functions in Single-Chip Modes (cont)

Pin	Selection of Pin Functions		
$P1_2$			
	$P1_2$DDR	0	1
	Pin function	Input	Output
$P1_1$ / E			
	$P1_1$DDR	0	1
	Pin function	Input	E clock output
$P1_0$ / ø			
	$P1_0$DDR	0	1
	Pin function	Input	ø clock output

9.3 Port 2

9.3.1 Overview

Port 2 is a five-bit input/output port with the pin configuration shown in figure 9-2. It functions as an input/output port only in the single-chip mode. In the expanded modes it is used for output of bus control signals.

Outputs from port 2 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair.

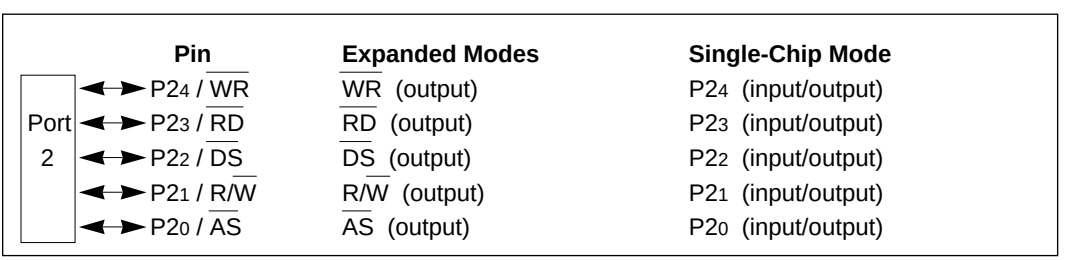

Figure 9-2 Pin Functions of Port 2

9.3.2 Port 2 Registers

Register Configuration: Table 9-5 lists the registers of port 2.

Table 9-5 Port 2 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 2 data direction register	P2DDR	W	H'E0	H'FF81
Port 2 data register	P2DR	R/W	H'E0	H'FF83

1. Port 2 Data Direction Register (P2DDR)—H'FF81

Bit	7	6	5	4	3	2	1	0
	—	—	—	$P2_4DDR$	$P2_3DDR$	$P2_2DDR$	$P2_1DDR$	$P2_0DDR$
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	W	W	W	W	W

P2DDR is an 8-bit register that selects the direction of each pin in port 2.

Single-Chip Mode: A pin functions as an output pin if the corresponding bit in P2DDR is set to “1,” and as an input pin if the bit is cleared to “0.”

Bits 4 to 0 can be written but not read. An attempt to read this register does not cause an error, but all bits are read as “1,” regardless of their true values.

Bits 7 to 5 are reserved. They cannot be modified and are always read as “1.”

At a reset and in the hardware standby mode, P2DDR is initialized to H'E0, making all five pins input pins. P2DDR is not initialized in the software standby mode, so if a P2DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 2 data register.

Expanded Modes: All bits of P2DDR are fixed at “1” and cannot be modified.

2. Port 2 Data Register (P2DR)—H'FF83

Bit	7	6	5	4	3	2	1	0
	—	—	—	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

P2DR is an 8-bit register containing the data for pins $P2_4$ to $P2_0$.

Bits 7 to 5 are reserved. They cannot be modified and are always read as “1.”

When the CPU reads P2DR, for output pins it reads the value in the P2DR latch, but for input pins, it obtains the pin status directly.

9.3.3 Pin Functions in Each Mode

Port 2 has different functions in the expanded modes (modes 1, 2, 3, 4) and the single-chip mode (mode 7). Separate descriptions are given below.

Pin Functions in Expanded Modes: In the expanded modes (modes 1, 2, 3, and 4), all pins of P2DDR is automatically set to “1” for output. Port 2 outputs the bus control signals ($\overline{AS}$, R/$\overline{W}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$).

Figure 9-3 shows the pin functions in the expanded modes.

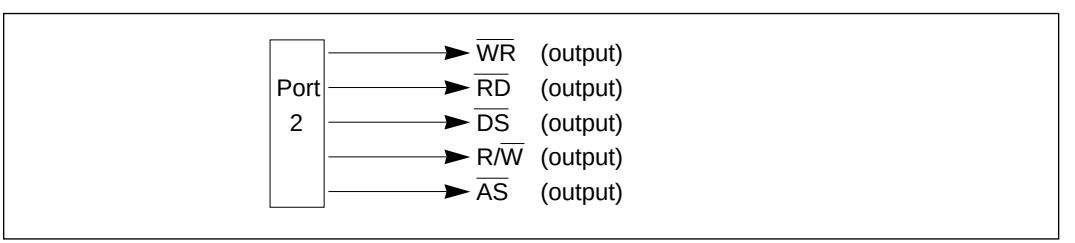

Figure 9-3 Port 2 Pin Functions in Expanded Modes

Pin Functions in Single-Chip Mode: In the single-chip mode (mode 7), each of the port 2 pins can be designated as an input pin or an output pin, as indicated in figure 9-4, by setting the corresponding bit in P2DDR to "1" for output or clearing it to "0" for input.

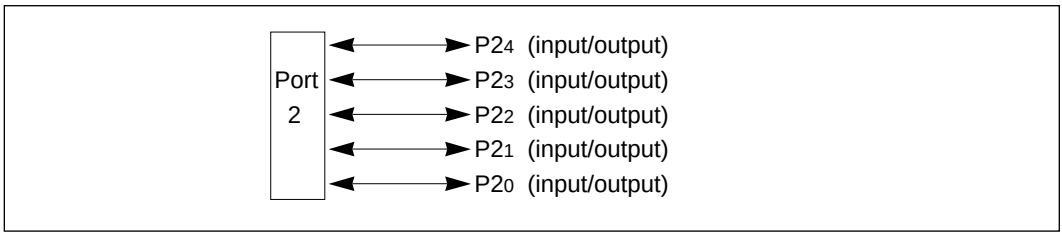

Figure 9-4 Port 2 Pin Functions in Single-Chip Mode

9.4 Port 3

9.4.1 Overview

Port 3 is an 8-bit input/output port with the pin configuration shown in figure 9-5. In the expanded modes it operates as the external data bus (D_7 – D_0). In the single-chip mode it operates as a general-purpose input/output port.

Outputs from port 3 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair.

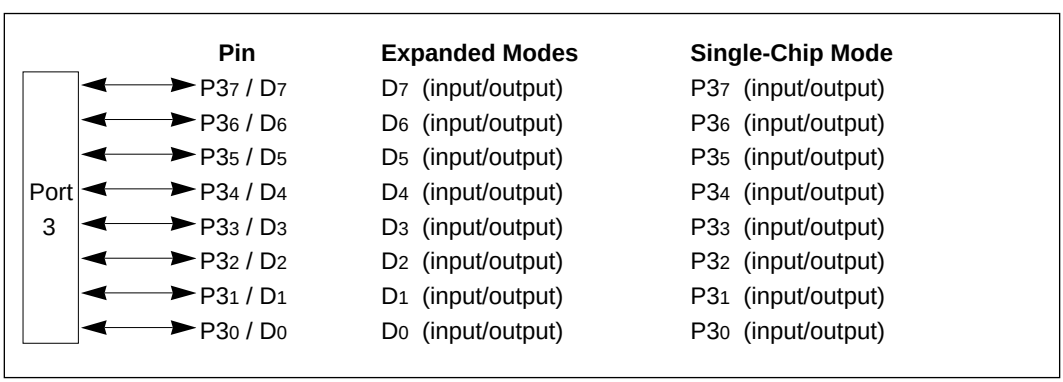

Figure 9-5 Pin Functions of Port 3

9.4.2 Port 3 Registers

Register Configuration: Table 9-6 lists the registers of port 3.

Table 9-6 Port 3 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 3 data direction register	P3DDR	W	H'00	H'FF84
Port 3 data register	P3DR	R/W	H'00	H'FF86

1. Port 3 Data Direction Register (P3DDR)—H'FF84

Bit	7	6	5	4	3	2	1	0
	$P3_7DDR$	$P3_6DDR$	$P3_5DDR$	$P3_4DDR$	$P3_3DDR$	$P3_2DDR$	$P3_1DDR$	$P3_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P3DDR is an 8-bit register that selects the direction of each pin in port 3.

Single-Chip Mode: A pin functions as an output pin if the corresponding bit in P3DDR is set to “1,” and as an input pin if the bit is cleared to “0.”

P3DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as “1,” regardless of their true values.

At a reset and in the hardware standby mode, P3DDR is initialized to H'00, making all eight pins input pins. P3DDR is not initialized in the software standby mode, so if a P3DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 3 data register.

Expanded Modes: P3DDR is not used.

2. Port 3 Data Register (P3DR)—H'FF86

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P3DR is an 8-bit register containing the data for pins $P3_7$ to $P3_0$.

At a reset and in the hardware standby mode, P3DR is initialized to H'00.

When the CPU reads P3DR, for output pins it reads the value in the P3DR latch, but for input pins, it obtains the pin status directly.

9.4.3 Pin Functions in Each Mode

Port 3 has different functions in the expanded modes (modes 1, 2, 3, 4) and the single-chip mode (mode 7). Separate descriptions are given below.

Pin Functions in Expanded Modes: In the expanded modes (modes 1, 2, 3, and 4), port 3 is automatically used as the data bus and P3DDR is ignored. Figure 9-6 shows the pin functions for the expanded modes.

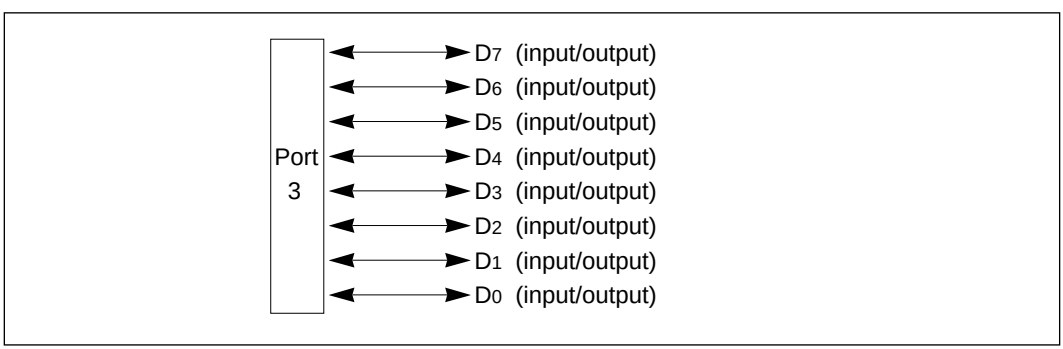

Figure 9-6 Port 3 Pin Functions in Expanded Modes

Pin Functions in Single-Chip Mode: In the single-chip mode (mode 7), each of the port 3 pins can be designated as an input pin or an output pin, as indicated in figure 9-7, by setting the corresponding bit in P3DDR to "1" for output or clearing it to "0" for input.

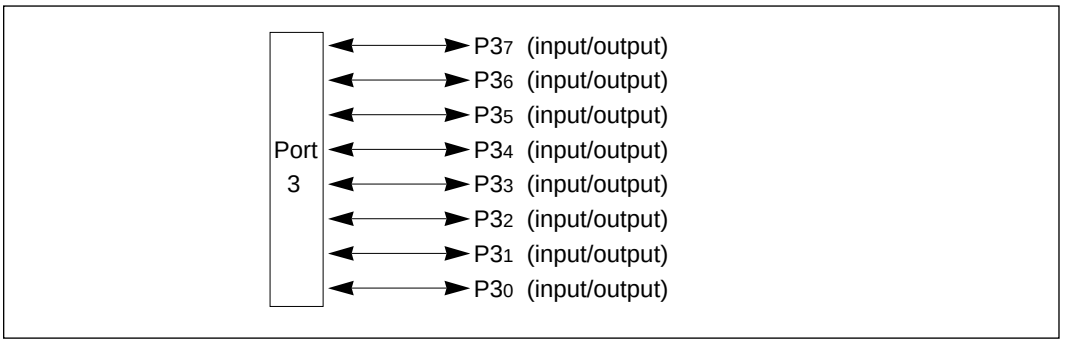

Figure 9-7 Port 3 Pin Functions in Single-Chip Mode

9.5 Port 4

9.5.1 Overview

Port 4 is an 8-bit input/output port with the pin configuration shown in figure 9-8. In the expanded modes it provides the low bits (A_7 – A_0) of the address bus. In the single-chip mode it operates as a general-purpose input/output port.

Outputs from port 4 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair or LED (with 8mA current sink).

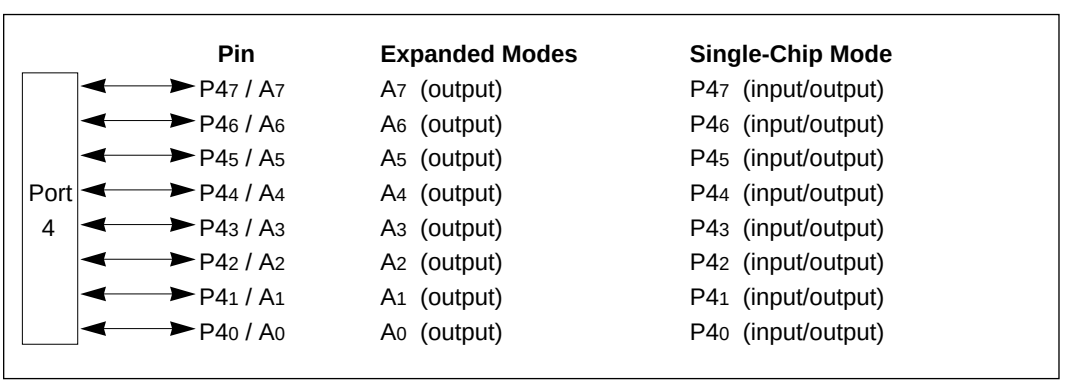

Figure 9-8 Pin Functions of Port 4

9.5.2 Port 4 Registers

Register Configuration: Table 9-7 lists the registers of port 4.

Table 9-7 Port 4 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 4 data direction register	P4DDR	W	H'00	H'FF85
Port 4 data register	P4DR	R/W	H'00	H'FF87

1. Port 4 Data Direction Register (P4DDR)—H'FF85

Bit	7	6	5	4	3	2	1	0
	$P4_7DDR$	$P4_6DDR$	$P4_5DDR$	$P4_4DDR$	$P4_3DDR$	$P4_2DDR$	$P4_1DDR$	$P4_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P4DDR is an 8-bit register that selects the direction of each pin in port 4.

Single-Chip Mode: A pin functions as an output pin if the corresponding bit in P4DDR is set to “1,” and as in input pin if the bit is cleared to “0.”

P4DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as “1,” regardless of their true values.

At a reset and in the hardware standby mode, P4DDR is initialized to H'00, making all eight pins input pins. P4DDR is not initialized in the software standby mode, so if a P4DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 4 data register.

Expanded Modes: All bits of P4DDR are fixed at “1” and cannot be modified.

2. Port 4 Data Register (P4DR)—H'FF87

Bit	7	6	5	4	3	2	1	0
	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P4DR is an 8-bit register containing the data for pins $P4_7$ to $P4_0$.

At a reset and in the hardware standby mode, P4DR is initialized to H'00.

When the CPU reads P4DR, for output pins it reads the value in the P4DR latch, but for input pins, it obtains the pin status directly.

9.5.3 Pin Functions in Each Mode

Port 4 has different functions in the expanded modes (modes 1, 2, 3, 4) and the single-chip mode (mode 7). Separate descriptions are given below.

Pin Functions in Expanded Modes: In the expanded modes (modes 1, 2, 3, and 4), port 4 is used for output of the low bits (A_7 – A_0) of the address bus. P4DDR is automatically set for output. Figure 9-9 shows the pin functions for the expanded modes.

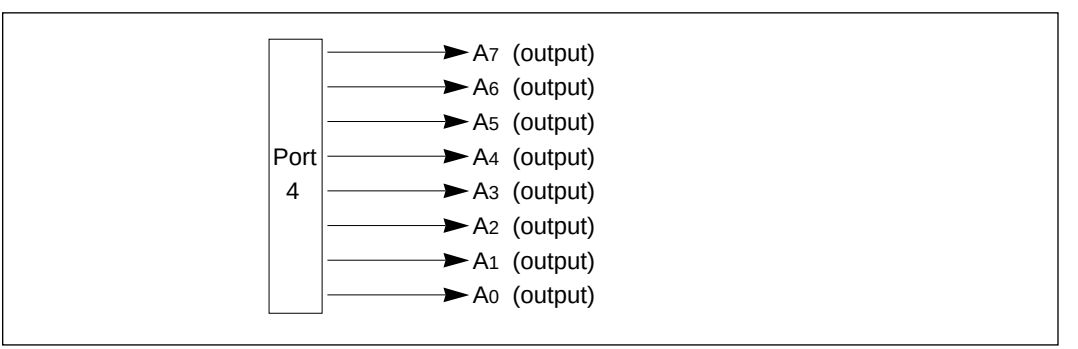

Figure 9-9 Port 4 Pin Functions in Expanded Modes

Pin Functions in Single-Chip Mode: In the single-chip mode (mode 7), each of the port 4 pins can be designated as an input pin or an output pin, as indicated in figure 9-10, by setting the corresponding bit in P4DDR to “1” for output or clearing it to “0” for input.

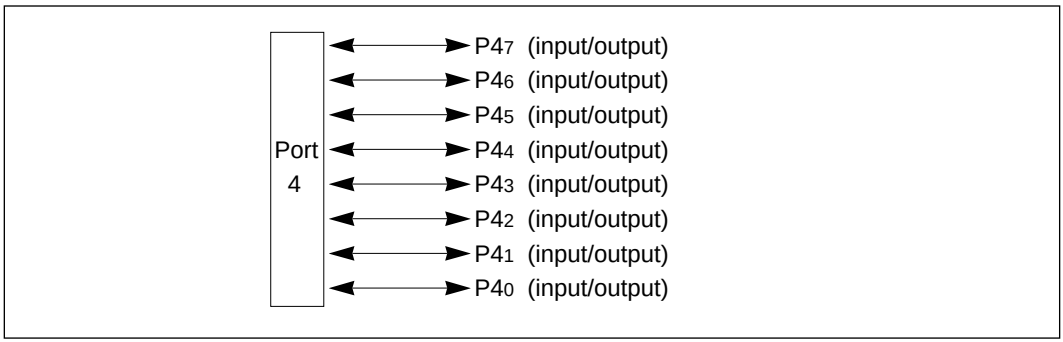

Figure 9-10 Port 4 Pin Functions in Single-Chip Mode

9.6 Port 5

9.6.1 Overview

Port 5 is an 8-bit input/output port with the pin configuration shown in figure 9-11. In the expanded modes that use the on-chip ROM (modes 2 and 4), the pins of port 5 function either as general-purpose input pins or as bits A_{15} – A_8 of the address bus, depending on the port 5 data direction register (P5DDR).

Port 5 has built-in MOS pull-ups that can be turned on or off under program control.

Outputs from port 5 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair.

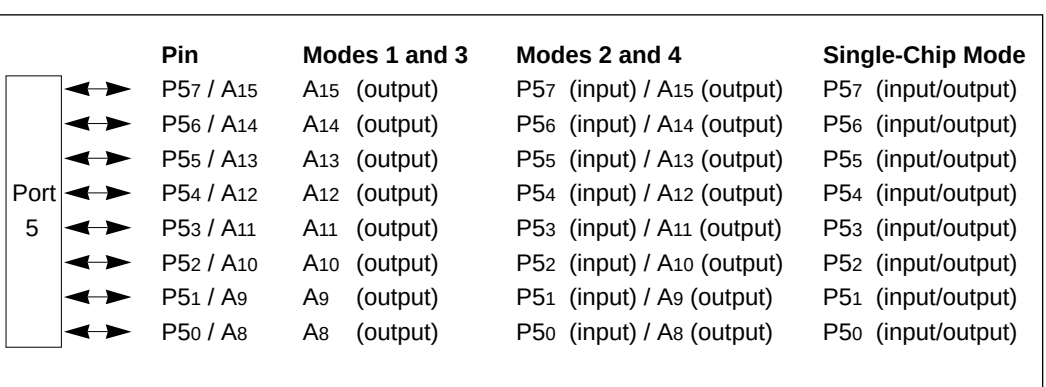

Figure 9-11 Pin Functions of Port 5

9.6.2 Port 5 Registers

Register Configuration: Table 9-8 lists the registers of port 5.

Table 9-8 Port 5 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 5 data direction register	P5DDR	W	H'00	H'FF88
Port 5 data register	P5DR	R/W	H'00	H'FF8A

1. Port 5 Data Direction Register (P5DDR)—H'FF88

Bit	7	6	5	4	3	2	1	0
	$P5_7$DDR	$P5_6$DDR	$P5_5$DDR	$P5_4$DDR	$P5_3$DDR	$P5_2$DDR	$P5_1$DDR	$P5_0$DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P5DDR is an 8-bit register that selects the direction of each pin in port 5.

Single-Chip Mode: A pin functions as an output pin if the corresponding bit in P5DDR is set to “1,” and as an input pin if the bit is cleared to “0.”

P5DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as “1,” regardless of their true values.

At a reset and in the hardware standby mode, P5DDR is initialized to H'00, making all eight pins input pins. P5DDR is not initialized in the software standby mode, so if a P5DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 5 data register.

Expanded Modes Using On-Chip ROM (Modes 2 and 4): If a “1” is set in P5DDR, the corresponding pin is used for address output. If a “0” is set in P5DDR, the pin is used for general-purpose input. P5DDR is initialized to H'00 at a reset and in the hardware standby mode.

Expanded Modes Not Using On-Chip ROM (Modes 1 and 3): All bits of P5DDR are fixed at “1” and cannot be modified.

Port 5 Data Register (P5DR)—H'FF8A

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P5DR is an 8-bit register containing the data for pins $P5_7$ to $P5_0$.

At a reset and in the hardware standby mode, P5DR is initialized to H'00.

When the CPU reads P5DR, for output pins it reads the value in the P5DR latch, but for input pins, it obtains the pin status directly.

9.6.3 Pin Functions in Each Mode

Port 5 operates in one way in modes 1 and 3, in another way in modes 2 and 4, and in a third way in mode 7. Separate descriptions are given below.

Pin Functions in Modes 1 and 3: In modes 1 and 3 (expanded modes in which the on-chip ROM is not used), all bits of P5DDR are automatically set to "1" for output, and the pins of port 5 carry bits A_{15} – A_8 of the address bus. Figure 9-12 shows the pin functions for modes 1 and 3.

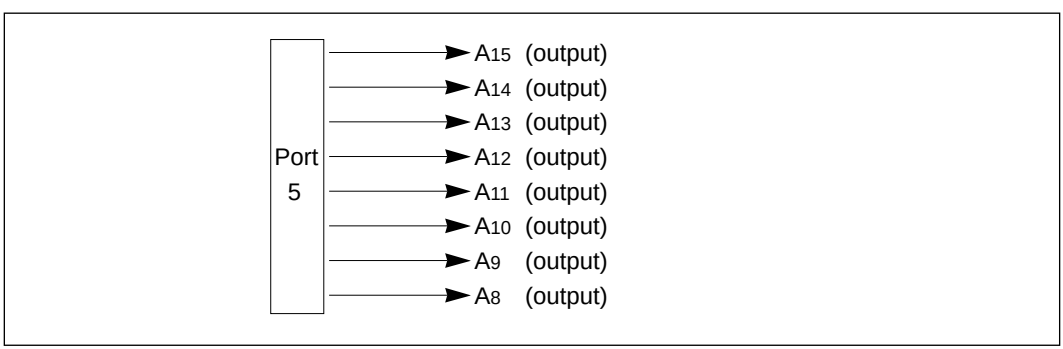

Figure 9-12 Port 5 Pin Functions in Modes 1 and 3

Pin Functions in Modes 2 and 4: In modes 2 and 4, (expanded modes in which the on-chip ROM is used), software can select whether to use port 5 for general-purpose input, or for output of bits A_{15} – A_8 of the address bus.

If a bit in P5DDR is set to "1," the corresponding pin is used for address output. If the bit is cleared to "0," the pin is used for input. A reset clears all P5DDR bits to "0," so before the address bus is used, all necessary bits in P5DDR must be set to "1."

Figure 9-13 shows the pin functions in modes 2 and 4.

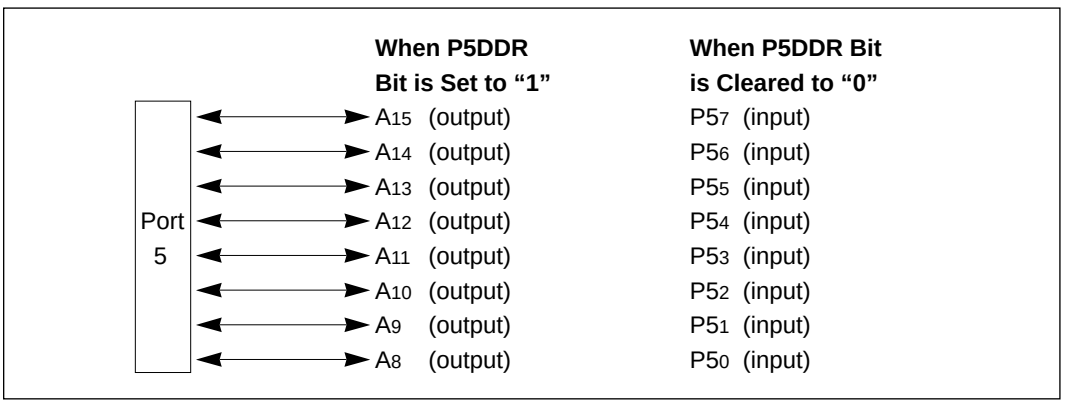

Figure 9-13 Port 5 Pin Functions in Modes 2 and 4

Pin Functions in Single-Chip Mode: In the single-chip mode (mode 7), each of the port 5 pins can be designated as an input pin or an output pin, as indicated in figure 9-14, by setting the corresponding bit in P5DDR to "1" for output or clearing it to "0" for input.

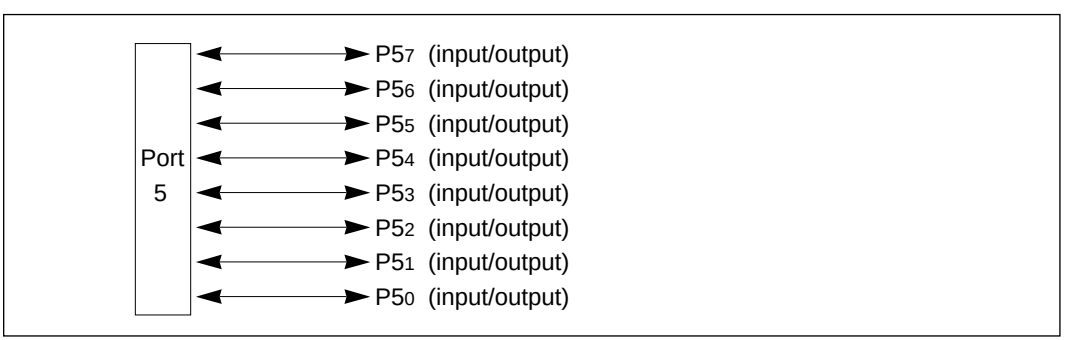

Figure 9-14 Port 5 Pin Functions in Single-Chip Mode

9.6.4 Built-In MOS Pull-Up

The MOS input pull-ups of port 5 are turned on by clearing the corresponding bit in P5DDR to "0" and writing a "1" in P5DR. These pull-ups are turned off at a reset and in the hardware standby mode. Table 9-9 indicates the status of the MOS pull-ups in various modes.

Table 9-9 Status of MOS Pull-Ups for Port 5

Mode	Reset	Hardware Standby Mode	Other Operating States*
1	OFF	OFF	OFF
2			ON/OFF
3			OFF
4			ON/OFF
7			

* Including the software standby mode.

Notation:
OFF: The MOS pull-up is always off.
ON/OFF: The MOS pull-up is on when P5DDR = 0 and P5DR = 1, and off otherwise.

Note on Usage of MOS Pull-Ups
If the bit manipulation instructions listed below are executed on input/output ports 5 and 6 which have selectable MOS pull-ups, the logic levels at input pins will be transferred to the DR latches, causing the MOS pull-ups to be unintentionally switched on or off.

This can occur with the following bit manipulation instructions: BSET, BCLR, BNOT

(1) Specific Example (BSET Instruction): An example will be shown in which the BSET instruction is executed for port 5 under the following conditions:
P5$_7$: Input pin, low, MOS pull-up transistor on
P5$_6$: Input pin, high, MOS pull-up transistor off
P5$_5$ – P5$_0$: Output pins, low

The intended purpose of this BSET instruction is to switch the output level at P5$_0$ from low to high.

A: Before Execution of BSET Instruction

	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low	High	Low	Low	Low	Low	Low	Low
DDR	0	0	1	1	1	1	1	1
DR	1	0	0	0	0	0	0	0
Pull-up	On	Off	Off	Off	Off	Off	Off	Off

B: Execution of BSET Instruction

```
BSET.B  #0      @PORT5
```

;set bit 0 in data register

C: After Execution of BSET Instruction

	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low	High	Low	Low	Low	Low	Low	High
DDR	0	0	1	1	1	1	1	1
DR	0	1	0	0	0	0	0	1
Pull-up	Off	On	Off	Off	Off	Off	Off	Off

Explanation: To execute the BSET instruction, the CPU begins by reading port 5. Since $P5_7$ and $P5_6$ are input pins, the CPU reads the level of these pins directly, not the value in the data register. It reads $P5_7$ as low (0) and $P5_6$ as high (1).

Since $P5_5$ to $P5_0$ are output pins, for these pins the CPU reads the value in the data register (0). The CPU therefore reads the value of port 5 as H'40, although the actual value in P5DR is H'80.

Next the CPU sets bit 0 of the read data to 1, changing the value to H'41.

Finally, the CPU writes this value (H'41) back to P5DR to complete the BSET instruction.

As a result, bit $P5_0$ is set to 1, switching pin $P5_0$ to high output. In addition, bits $P5_7$ and $P5_6$ are both modified, changing the on/off settings of the MOS pull-up transistors of pins $P5_7$ and $P5_6$.

Programming Solution: The switching of the pull-ups for $P5_7$ and $P5_6$ in the preceding example can be avoided by using a byte in RAM as a work area for P5DR, performing bit manipulations on the work area, then writing the result to P5DR.

A: Before Execution of BSET Instruction

```
MOV.B   #80, R0          ;write data (H'80) for data register
MOV.B   R0,  @RAM0       ;write to work area (RAM0)
MOV.B   R0,  @PORT5      ;write to P5DR
```

	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low	High	Low	Low	Low	Low	Low	Low
DDR	0	0	1	1	1	1	1	1
DR	1	0	0	0	0	0	0	0
Pull-up	On	Off	Off	Off	Off	Off	Off	Off
RAM0	1	0	0	0	0	0	0	0

B: Execution of BSET Instruction

```
BSET.B   #0, @RAM0       ;set bit 0 in work area (RAM0)
```

C: After Execution of BSET Instruction

```
MOV.B  @RAM0, R0         ;get value in work area (RAM0)
MOV.B  R0,    @PORT5     ;write value to P5DR
```

	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low	High	Low	Low	Low	Low	Low	High
DDR	0	0	1	1	1	1	1	1
DR	1	0	0	0	0	0	0	1
Pull-up	On	Off	Off	Off	Off	Off	Off	Off
RAM0	1	0	0	0	0	0	0	0

9.7 Port 6

9.7.1 Overview

Port 6 is a 4-bit input/output port with the pin configuration shown in figure 9-15. In mode 4 (the expanded maximum mode that uses the on-chip ROM), the pins of port 6 function either as general-purpose input pins or as the page address bus, depending on the port 6 data direction register (P6DDR).

Port 6 has built-in MOS pull-ups that can be turned on or off under program control.

Outputs from port 6 can drive one TTL load and a 90pF capacitive load. They can also drive a Darlington transistor pair.

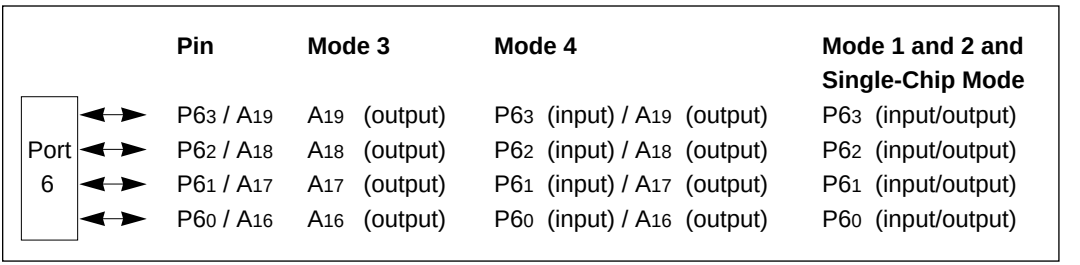

Figure 9-15 Pin Functions of Port 6

9.7.2 Port 6 Registers

Register Configuration: Table 9-10 lists the registers of port 6.

Table 9-10 Port 6 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 6 data direction register	P6DDR	W	H'F0	H'FF89
Port 6 data register	P6DR	R/W	H'F0	H'FF8B

1. Port 6 Data Direction Register (P6DDR)—H'FF89

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	P63DDR	P62DDR	P61DDR	P60DDR
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	W	W	W	W

P6DDR is an 8-bit register that selects the direction of each pin in port 6.

Single-Chip Mode and Expanded Minimum Modes: A pin functions as an output pin if the corresponding bit in P6DDR is set to “1,” and as an input pin if the bit is cleared to “0.”

Bits 3 to 0 can be written but not read. An attempt to read these bits does not cause an error, but all bits are read as “1,” regardless of their true values.

Bits 7 to 4 are reserved. They cannot be modified and are always read as “1.”

At a reset and in the hardware standby mode, P6DDR is initialized to H'F0, making all four pins input pins. P6DDR is not initialized in the software standby mode, so in the single-chip mode, or expanded minimum mode, if a P6DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 6 data register.

Expanded Maximum Mode Using On-Chip ROM (Mode 4): If a “1” is set in P6DDR, the corresponding pin is used for address output. If a “0” is set in P6DDR, the pin is used for input. P6DDR is initialized to H'F0 at a reset and in the hardware standby mode.

Expanded Maximum Mode Not Using On-Chip ROM (Mode 3): All bits of P6DDR are fixed at “1” and cannot be modified.

2. Port 6 Data Register (P6DR)—H'FF8B

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

P6DR is an 8-bit register containing the data for pins $P6_3$ to $P6_0$.

Bits 7 to 4 are reserved. They cannot be modified and are always read as “1.”

At a reset and in the hardware standby mode, P6DR is initialized to H'F0.

When the CPU reads P6DR, for output pins it reads the value in the P6DR latch, but for input pins, it obtains the pin status directly.

9.7.3 Pin Functions in Each Mode

The usage of port 6 depends on the MCU operating mode. Separate descriptions are given below.

Pin Functions in Mode 3: In mode 3 (the expanded maximum mode in which the on-chip ROM is not used), P6DDR is automatically set for output, and the pins of port 6 carry the page address bits (A_{19} – A_{16}) of the address bus. Figure 9-16 shows the pin functions for mode 3.

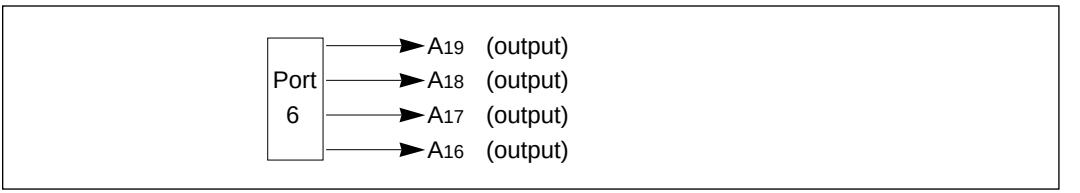

Figure 9-16 Port 6 Pin Functions in Mode 3

Pin Functions in Mode 4: In mode 4, (the expanded maximum mode in which the on-chip ROM is used), software can select whether to use port 6 for general-purpose input, or for output of the page address bits.

If a bit in P6DDR is set to "1," the corresponding pin is used for page address output. If the bit is cleared to "0," the pin is used for input. A reset initializes these pins to the general-purpose input function, so when the address bus is used, all necessary bits in P6DDR must first be set to "1."

Figure 9-17 shows the pin functions in mode 4.

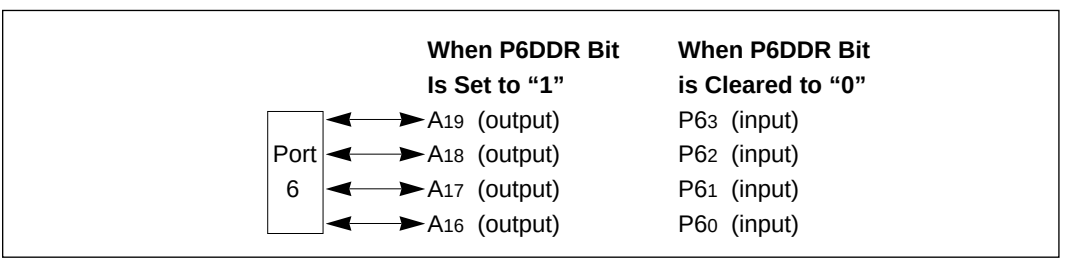

Figure 9-17 Port 6 Pin Functions in Mode 4

Pin Functions in Single-Chip Mode and Expanded Minimum Modes: In the single-chip mode (mode 7) and expanded minimum modes (modes 1 and 2), each of the port 6 pins can be designated as an input pin or an output pin, as indicated in figure 9-18, by setting the corresponding bit in P6DDR to "1" for output or clearing it to "0" for input.

Figure 9-18 Port 6 Pin Functions in Modes 7, 2, and 1

9.7.4 Built-in MOS Pull-Up

Port 6 has programmable MOS input pull-ups which are turned on by clearing the corresponding bit in P6DDR to "0" and writing a "1" in P6DR. These pull-ups are turned off at a reset and in the hardware standby mode. Table 9-11 indicates the status of the MOS pull-ups in various modes.

Table 9-11 Status of MOS Pull-Ups for Port 5

Mode	Reset	Hardware Standby Mode	Other Operating States*
1	OFF	OFF	ON/OFF
2			
3			OFF
4			ON/OFF
7			

* Including the software standby mode.

Notation:
OFF: The MOS pull-up is always off.
ON/OFF: The MOS pull-up is on when P6DDR = 0 and P6DR = 1, and off otherwise.

Note: When using the built-in pull-ups, see the "Note on Usage of MOS Pull-Ups" in section 9.6.4.

9.8 Port 7

9.8.1 Overview

Port 7 is an 8-bit input/output port with the pin configuration shown in figure 9-19. Its pins also carry input and output signals for the on-chip free-running timers (FRT1, FRT2, and FRT3), and two input signals for the on-chip 8-bit timer.

Port 7 has Schmitt inputs. Outputs from port 7 can drive one TTL load and a 30pF capacitive load. They can also drive a Darlington transistor pair.

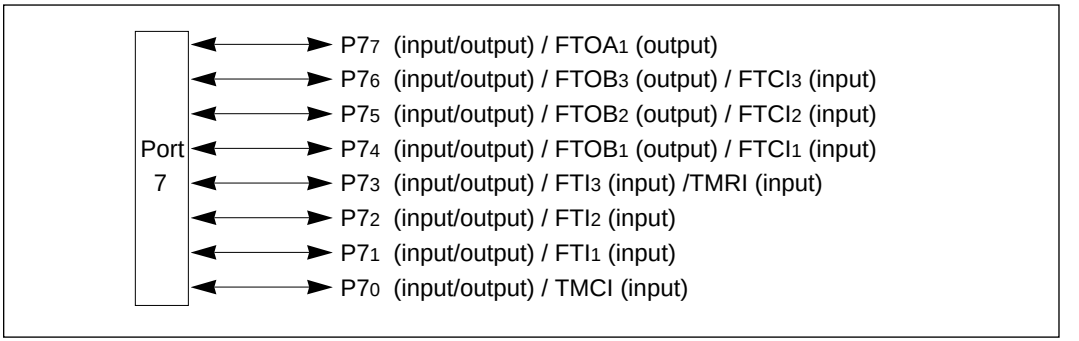

Figure 9-19 Pin Functions of Port 7

9.8.2 Port 7 Registers

Register Configuration: Table 9-12 lists the registers of port 7.

Table 9-12 Port 7 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 7 data direction register	P7DDR	W	H'00	H'FF8C
Port 7 data register	P7DR	R/W	H'00	H'FF8E

1. Port 7 Data Direction Register (P7DDR)—H'FF8C

Bit	7	6	5	4	3	2	1	0
	P77DDR	P76DDR	P75DDR	P74DDR	P73DDR	P72DDR	P71DDR	P70DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P7DDR is an 8-bit register that selects the direction of each pin in port 7. A pin functions as an output pin if the corresponding bit in P7DDR is set to “1,” and as an input pin if the bit is cleared to “0.”

P7DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as “1,” regardless of their true values.
At a reset and in the hardware standby mode, P7DDR is initialized to H'00, setting all pins for input. P7DDR is not initialized in the software standby mode, so if a P7DDR bit is set to “1” when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 7 data register.

A transition to the software standby mode initializes the on-chip supporting modules, so any pins of port 7 that were being used by an on-chip timer when the transition occurs revert to general-purpose input or output, controlled by P7DDR and P7DR.

2. Port 7 Data Register (P7DR)—H'FF8E

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P7DR is an 8-bit register containing the data for pins $P7_7$ to $P7_0$. When the CPU reads P7DR, for output pins it reads the value in the P7DR latch, but for input pins, it obtains the pin status directly.

9.8.3 Pin Functions

The pin functions of port 7 are the same in all MCU operating modes. As figure 9-19 indicated, these pins are used for input and output of on-chip timer signals as well as for general-purpose input and output. For some pins, two or more functions can be enabled simultaneously.

$P7_7$ can be used either for general-purpose input/output, or as the output pin for the output compare A signal (FTOA) from free-running timer 1.

$P7_6$ to $P7_4$ can be used either for general-purpose input/output, or as the output pins for the output compare B signals (FTOB) from free-running timers 3 to 1. When used for general-purpose input and output, they can also provide external clock input (FTCI) to the free-running counters. This additional function is selected when the clock select 1 and 0 bits (CKS1 and CKS0) in the free-running timer control registers are both set to “1.”

$P7_3$ to $P7_1$ function simultaneously as general-purpose input/output pins and as input pins for the input capture signals (FTI) of free-running timers 3 to 1.

P7$_3$ and P7$_0$ can be used for timer reset input (TMRI) and timer clock input (TMCI) for the 8-bit timer, as well as for general-purpose input and output.

Table 9-13 shows how the functions of the pins of port 7 are selected.

Table 9-13 Port 7 Pin Functions

Pin — **Selection of Pin Functions**

P7$_7$ / FTOA$_1$ — The function depends on the output enable A bit (OEA) of the FRT1 timer control register (TCR) and on the P7$_7$DDR bit as follows:

OEA	0		1	
P7$_7$DDR	0	1	0	1
Pin function	P7$_7$ input	P7$_7$ output	FTOA$_1$ output	

P7$_6$ / FTOB$_3$ / FTCI$_3$ — The function depends on the output compare B bit (OEB) of the FRT3 timer control register (TCR) and on the P7$_6$DDR bit as follows:

OEB	0		1	
P7$_6$DDR	0	1	0	1
Pin function	P7$_6$ input	P7$_6$ output	FTOB$_3$ output	
	FTCI$_3$ input			

P7$_5$ / FTOB$_2$ / FTCI$_2$ — The function depends on the output compare B bit (OEB) of the FRT2 timer control register (TCR) and on the P7$_5$DDR bit as follows:

OEB	0		1	
P7$_5$DDR	0	1	0	1
Pin function	P7$_5$ input	P7$_5$ output	FTOB$_2$ output	
	FTCI$_2$ input			

P7$_4$ / FTOB$_1$ / FTCI$_1$ — The function depends on the output compare B bit (OEB) of the FRT1 timer control register (TCR) and on the P7$_4$DDR bit as follows:

OEB	0		1	
P7$_4$DDR	0	1	0	1
Pin function	P7$_4$ input	P7$_4$ output	FTOB$_1$ output	
	FTCI$_1$ input			

Table 9-13 Port 7 Pin Functions (cont)

Pin	Selection of Pin Functions
$P7_3$ / FTI_3 / TMRI	The function depends on the counter clear bits 1 and 0 (CCLR1 and CCLR0) in the timer control register (TCR) of the 8-bit timer, and on the $P7_3$DDR bit as follows: CCLR1, CCLR0: At least one bit is “0.” Both bits are set to “1”

$P7_3$DDR	0	1
Pin function	$P7_3$ input	$P7_3$ output
	FTI_3 input and TMRI input	

$P7_2$ / FTI_2

$P7_2$DDR	0	1
Pin function	$P7_2$ input	$P7_2$ output
	FTI_2 input	

$P7_1$ / FTI_1

$P7_1$DDR	0	1
Pin function	$P7_1$ input	$P7_1$ output
	FTI_1 input	

$P7_0$ / TMCI — This pin always has a general-purpose input/output function, and can simultaneously be used for external clock input for the 8-bit timer, depending on clock select bits 2 to 0 (CKS2, CKS1, and CKS0) in the timer control register (TCR). See section 11, “8-bit Timer” for details.

$P7_0$DDR	0	1
Pin function	$P7_0$ input	$P7_0$ output
	TMCI input	

9.9 Port 8

9.9.1 Overview

Port 8 is an 8-bit input port that also receives inputs for the on-chip A/D converter. The pin functions are the same in all MCU operating modes, as shown in figure 9-20.

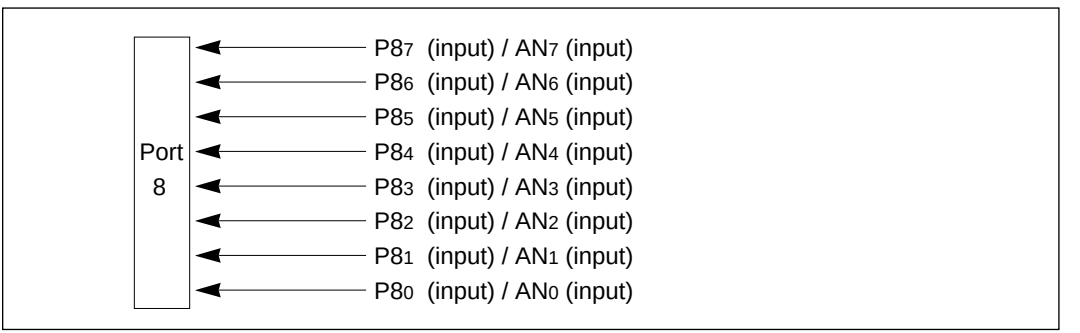

Figure 9-20 Pin Functions of Port 8

9.9.2 Port 8 Registers

Register Configuration: Port 8 has only the data register described in table 9-14. Since it is exclusively an input port, there is no data direction register.

Table 9-14 Port 8 Registers

Name	Abbreviation	Read/Write	Address
Port 8 data register	P8DR	R	H'FF8F

1. Port 8 Data Register (P8DR)—H'FF8F

Bit	7	6	5	4	3	2	1	0
	$P8_7$	$P8_6$	$P8_5$	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

When the CPU reads P8DR it always reads the current status of each pin, except that during A/D conversion the pin currently being converted reads “1” regardless of the actual input voltage at that pin.

9.10 Port 9

9.10.1 Overview

Port 9 is an 8-bit input/output port with the pin configuration shown in figure 9-21. In addition to general-purpose input and output, its pins are used for the output compare A signals from free-running timers 2 and 3, for PWM timer output, and for input and output by the on-chip serial communication interface 9 (SCI). The pin functions are the same in all MCU operating modes.

Outputs from port 9 can drive one TTL load and a 30pF capacitive load. They can also drive a Darlington transistor pair.

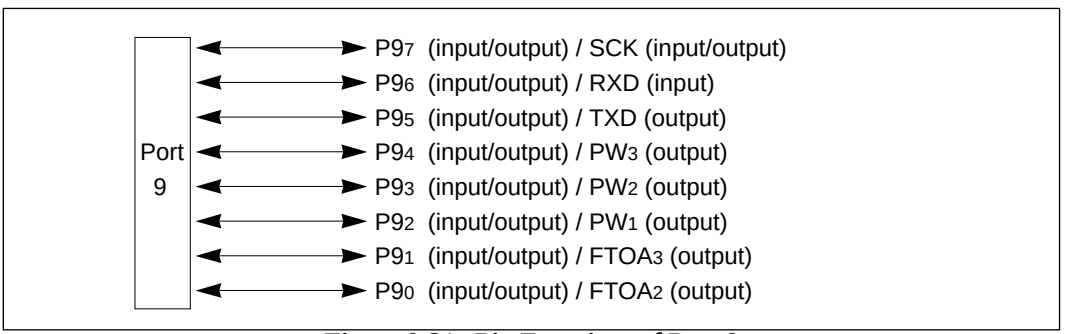

Figure 9-21 Pin Functions of Port 9

9.10.2 Port 9 Registers

Register Configuration: Table 9-15 lists the registers of port 9.

Table 9-15 Port 9 Registers

Name	Abbreviation	Read/Write	Initial Value	Address
Port 9 data direction register	P9DDR	W	H'00	H'FFFE
Port 9 data register	P9DR	R/W	H'00	H'FFFF

1. Port 9 Data Direction Register (P9DDR)—H'FFFE

Bit	7	6	5	4	3	2	1	0
	$P9_7DDR$	$P9_6DDR$	$P9_5DDR$	$P9_4DDR$	$P9_3DDR$	$P9_2DDR$	$P9_1DDR$	$P9_0DDR$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

P9DDR is an 8-bit register that selects the direction of each pin in port 9. A pin functions as an output pin if the corresponding bit in P9DDR is set to "1," and as an input pin if the bit is cleared to "0."

P9DDR can be written but not read. An attempt to read this register does not cause an error, but all bits are read as "1," regardless of their true values.

At a reset and in the hardware standby mode, P9DDR is initialized to H'00, setting all pins for input. P9DDR is not initialized in the software standby mode, so if a P9DDR bit is set to "1" when the chip enters the software standby mode, the corresponding pin continues to output the value in the port 9 data register.

A transition to the software standby mode initializes the on-chip supporting modules, so any pins of port 9 that were being used by an on-chip module (example: free-running timer output) when the transition occurs revert to general-purpose input or output, controlled by P9DDR and P9DR.

2. Port 9 Data Register (P9DR)—H'FFFF

Bit	7	6	5	4	3	2	1	0
	$P9_7$	$P9_6$	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P9DR is an 8-bit register containing the data for pins $P9_7$ to $P9_0$. When the CPU reads P9DR, for output pins it reads the value in the P9DR latch, but for input pins, it obtains the pin status directly.

9.10.3 Pin Functions

The pin functions of port 9 are the same in all MCU operating modes. As figure 9-21 indicated, these pins are used for output of on-chip timer signals and for input and output of serial data and clock signals as well as for general-purpose input and output. Specifically, they carry output signals for free-running timers 2 and 3, output signals for the pulse-width modulation (PWM) timer, and input and output signals for the serial communication interface.

Table 9-16 shows how the functions of the pins of port 9 are selected.

Table 9-16 Port 9 Pin Functions

Pin	Selection of Pin Functions
$P9_7$ / SCK	The function depends on the communication mode bit (C/$\overline{A}$) and the clock enable 1 and 2 bits (CKE1 and CKE0) of the serial control register (SCR) of the serial communication interface as follows:

C/$\overline{A}$	0				1			
CKE1	0		1		0		1	
CKE0	0	1	0	1	0	1	0	1
Pin function	$P9_7$ input or output*	SCI internal clock output	SCI external clock input		SCI internal clock output		SCI external clock input	

* Input or output is selected by the $P9_7$DDR bit.

$P9_6$ / RXD — The function depends on the receive enable bit (RE) of the serial control register (SCR) and on the $P9_6$DDR bit as follows:

RE	0		1	
$P9_6$DDR	0	1	0	1
Pin function	$P9_6$ input	$P9_6$ output	RXD input	

$P9_5$ / TXD — The function depends on the transmit enable bit (TE) of the serial control register (SCR) and on the $P9_5$DDR bit as follows:

TE	0		1	
$P9_5$DDR	0	1	0	1
Pin function	$P9_5$ input	$P9_5$ output	TXD output	

Table 9-16 Port 9 Pin Functions (cont)

Pin	Selection of Pin Functions
$P9_4$ / PW_3	The function depends on the output enable bit (OE) of the timer control register of PWM timer channel 3 and on the $P9_4$DDR bit as follows:

OE	0		1	
$P9_4$DDR	0	1	0	1
Pin function	$P9_4$ input	$P9_4$ output	PW_3 output	

$P9_3$ / PW_2	The function depends on the output enable bit (OE) of the timer control register of PWM timer channel 2 and on the $P9_3$DDR bit as follows:

OE	0		1	
$P9_3$DDR	0	1	0	1
Pin function	$P9_3$ input	$P9_3$ output	PW_2 output	

$P9_2$ / PW_1	The function depends on the output enable bit (OE) of the timer control register of PWM timer channel 1 and on the $P9_2$DDR bit as follows:

OE	0		1	
$P9_2$DDR	0	1	0	1
Pin function	$P9_2$ input	$P9_2$ output	PW_1 output	

$P9_1$ / $FTOA_3$	The function depends on the output compare A bit (OEA) of the FRT3 timer control $FTOA_3$ register (TCR) and on the $P9_1$DDR bit as follows:

OEA	0		1	
$P9_1$DDR	0	1	0	1
Pin function	$P9_1$ input	$P9_1$ output	$FTOA_3$ output	

$P9_0$ / $FTOA_2$	The function depends on the output compare A bit (OEA) of the FRT3 timer control $FTOA_2$ register (TCR) and on the $P9_0$DDR bit as follows:

OEA	0		1	
$P9_0$DDR	0	1	0	1
Pin function	$P9_0$ input	$P9_0$ output	$FTOA_2$ output	