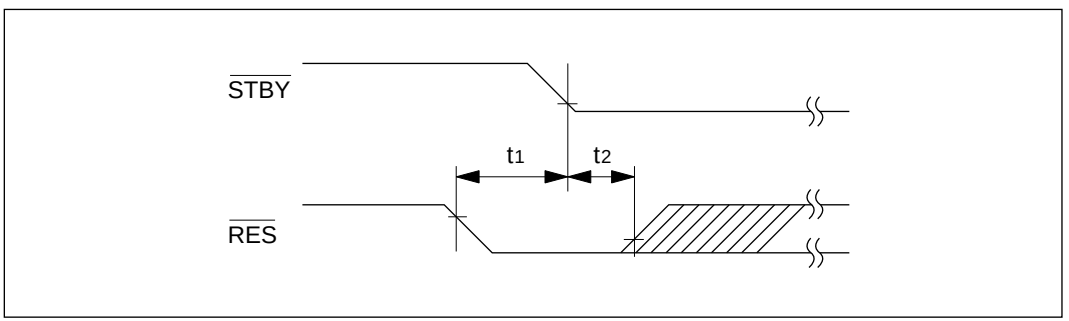
# Appendix F Timing of Entry to and Recovery from Hardware Standby Mode

**Timing of Entry to Hardware Standby Mode**

(1) To preserve RAM contents, drive the $\overline{\text{RES}}$ signal line low 10 system clock cycles before the fall of the $\overline{\text{STBY}}$ signal.
The $\overline{\text{RES}}$ signal can rise any time after $\overline{\text{STBY}}$ goes low. The minimum necessary time from $\overline{\text{STBY}}$ low to RES high is 0 ns.




(2) When it is not necessary to preserve RAM contents, $\overline{\text{RES}}$ need not be driven low as in (1).

**Timing of Exit from Hardware Standby Mode**

Drive the $\overline{\text{RES}}$ signal line low approximately 100 ns before the rise of the $\overline{\text{STBY}}$ signal.