Section 10 16-Bit Free-Running Timers

10.1 Overview

The H8/532 has an on-chip 16-bit free-running timer (FRT) module with three independent channels (FRT1, FRT2, and FRT3). All three channels are functionally identical.

Each channel has a 16-bit free-running counter that it uses as a time base. Applications of the FRT module include rectangular-wave output (up to two independent waveforms per channel), input pulse width measurement, and measurement of external clock periods.

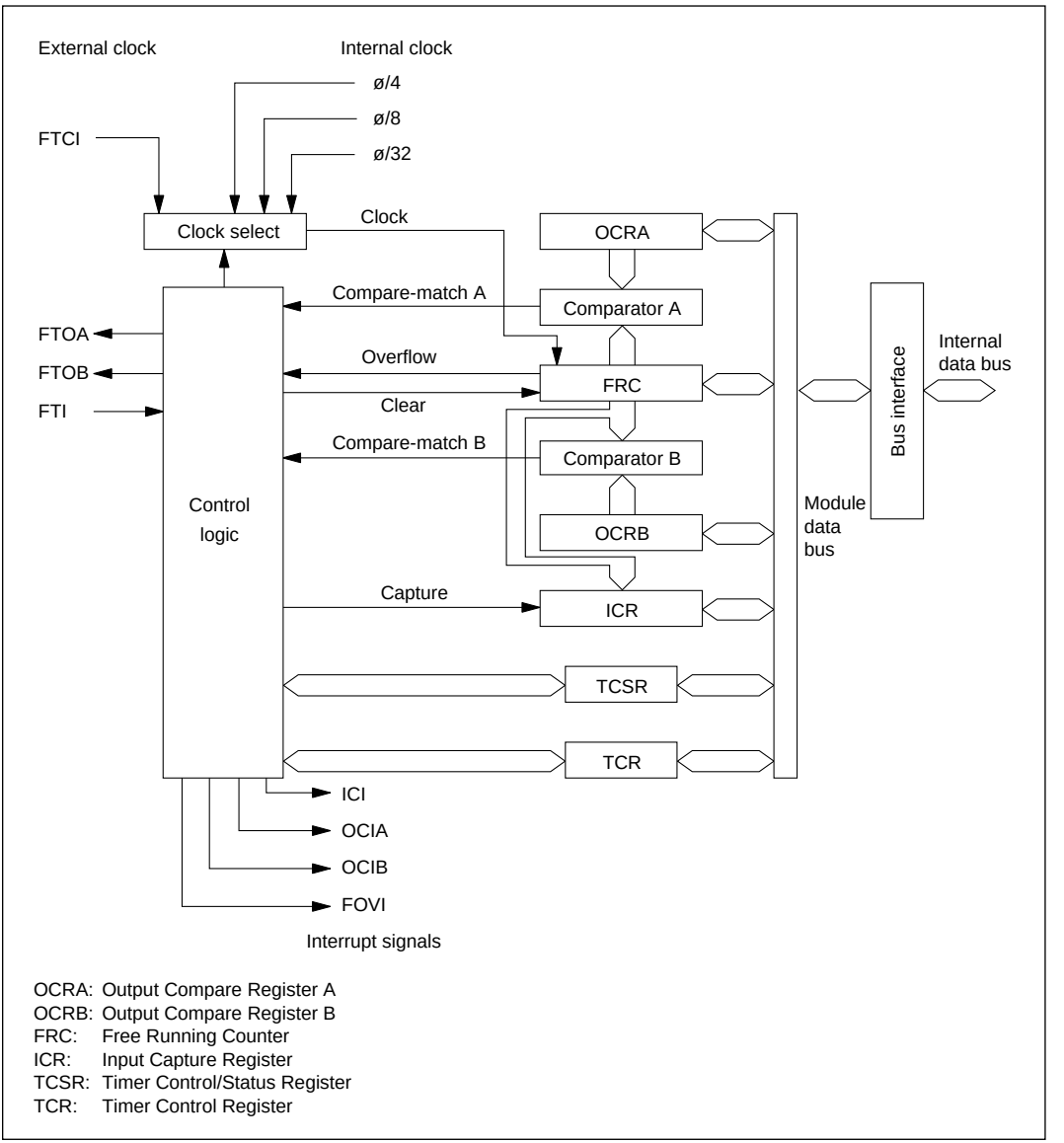
10.1.1 Features

The features of the free-running timer module are listed below.

- Selection of four clock sources
  The free-running counters can be driven by an internal clock source (ø/4, ø/8, or ø/32), or an external clock input (enabling use as an external event counter).
- Two independent comparators
  Each free-running timer channel can generate two independent waveforms.
- Input capture function
  The current count can be captured on the rising or falling edge (selectable) of an input signal.
- Four types of interrupts
  Compare-match A and B, input capture, and overflow interrupts can be requested independently.
  The compare-match and input capture interrupts can be served by the data transfer controller (DTC), enabling interrupt-driven data transfer with minimal CPU programming.
- Counter can be cleared under program control
  The free-running counters can be cleared on compare-match A.

10.1.2. Block Diagram

Figure 10-1 shows a block diagram of one free-running timer channel.



OCRA: Output Compare Register A
OCRB: Output Compare Register B
FRC: Free Running Counter
ICR: Input Capture Register
TCSR: Timer Control/Status Register
TCR: Timer Control Register

Figure 10-1 Block Diagram of 16-Bit Free-Running Timer

10.1.3 Input and Output Pins

Table 10-1 lists the input and output pins of the free-running timer module.

Table 10-1 Input and Output Pins of Free-Running Timer Module

Channel	Name	Abbreviation	I/O	Function
1	Output compare A	$FTOA_1$	Output	Output controlled by comparator A of FRT1
	Output compare B or counter clock input	$FTOB_1$ / $FTCI_1$	Output / Input	Output controlled by comparator B of FRT1, or input of external clock source for FRT1
	Input capture	FTI_1	Input	Trigger for capturing current count of FRT1
2	Output compare A	$FTOA_2$	Output	Output controlled by comparator A of FRT2
	Output compare B or counter clock input	$FTOB_2$ / $FTCI_2$	Output / Input	Output controlled by comparator B of FRT2, or input of external clock source for FRT2
	Input capture	FTI_2	Input	Trigger for capturing current count of FRT2
3	Output compare A	$FTOA_3$	Output	Output controlled by comparator A of FRT3
	Output compare B or counter clock input	$FTOB_3$ / $FTCI_3$	Output / Input	Output controlled by comparator B of FRT3, or input of external clock source for FRT3
	Input capture	FTI_3	Input	Trigger for capturing current count of FRT3

10.1.4 Register Configuration

Table 10-2 lists the registers of each free-running timer channel.

Table 10-2 Register Configuration

Channel	Name	Abbreviation	R/W	Initial Value	Address
	Timer control register	TCR	R/W	H'00	H'FF90
	Timer control/status register	TCSR	R/(W)*	H'00	H'FF91
	Free-running counter (High)	FRC (H)	R/W	H'00	H'FF92
	Free-running counter (Low)	FRC (L)	R/W	H'00	H'FF93
1	Output compare register A (High)	OCRA (H)	R/W	H'FF	H'FF94
	Output compare register A (Low)	OCRA (L)	R/W	H'FF	H'FF95
	Output compare register B (High)	OCRB (H)	R/W	H'FF	H'FF96
	Output compare register B (Low)	OCRB (L)	R/W	H'FF	H'FF97
	Input capture register (High)	ICR (H)	R	H'00	H'FF98
	Input capture register (Low)	ICR (L)	R	H'00	H'FF99
	Timer control register	TCR	R/W	H'00	H'FFA0
	Timer control/status register	TCSR	R/(W)*	H'00	H'FFA1
	Free-running counter (High)	FRC (H)	R/W	H'00	H'FFA2
	Free-running counter (Low)	FRC (L)	R/W	H'00	H'FFA3
2	Output compare register A (High)	OCRA (H)	R/W	H'FF	H'FFA4
	Output compare register A (Low)	OCRA (L)	R/W	H'FF	H'FFA5
	Output compare register B (High)	OCRB (H)	R/W	H'FF	H'FFA6
	Output compare register B (Low)	OCRB (L)	R/W	H'FF	H'FFA7
	Input capture register (High)	ICR (H)	R	H'00	H'FFA8
	Input capture register (Low)	ICR (L)	R	H'00	H'FFA9

* Software can write a “0” to clear bits 7 to 4, but cannot write a “1” in these bits.

Table 10-2 Register Configuration (cont)

Channel	Name	Abbreviation	R/W	Initial Value	Address
	Timer control register	TCR	R/W	H'00	H'FFB0
	Timer control/status register	TCSR	R/(W)*	H'00	H'FFB1
	Free-running counter (High)	FRC (H)	R/W	H'00	H'FFB2
	Free-running counter (Low)	FRC (L)	R/W	H'00	H'FFB3
3	Output compare register A (High)	OCRA (H)	R/W	H'FF	H'FFB4
	Output compare register A (Low)	OCRA (L)	R/W	H'FF	H'FFB5
	Output compare register B (High)	OCRB (H)	R/W	H'FF	H'FFB6
	Output compare register B (Low)	OCRB (L)	R/W	H'FF	H'FFB7
	Input capture register (High)	ICR (H)	R	H'00	H'FFB8
	Input capture register (Low)	ICR (L)	R	H'00	H'FFB9

* Software can write a “0” to clear bits 7 to 4, but cannot write a “1” in these bits.

10.2 Register Descriptions

10.2.1 Free-Running Counter (FRC)—H'FF92, H'FFA2, H'FFB2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each FRC is a 16-bit readable/writable up-counter that increments on an internal pulse generated from a clock source. The clock source is selected by the clock select 1 and 0 bits (CKS1 and CKS0) of the timer control register (TCR).

The FRC can be cleared by compare-match A.

When the FRC overflows from H'FFFF to H'0000, the overflow flag (OVF) in the timer control/status register (TCSR) is set to “1.”

Because the FRC is a 16-bit register, a temporary register (TEMP) is used when the FRC is written or read. See section 10.3, “CPU Interface” for details.

The FRCs are initialized to H'0000 at a reset and in the standby modes.

10.2.2 Output Compare Registers A and B (OCRA and OCRB)—H'FF94 and H'FF96, H'FFA4 and H'FFA6, H'FFB4 and H'FFB6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OCRA and OCRB are 16-bit readable/writable registers, the contents of which are continually compared with the value in the FRC. When a match is detected, the corresponding output compare flag (OCFA or OCFB) is set in the timer control/status register (TCSR).

In addition, if the output enable bit (OEA or OEB) in the timer control register (TCR) is set to "1," when the output compare register and FRC values match, the logic level selected by the output level bit (OLVLA or OLVLB) in the timer control status register (TCSR) is output at the output compare pin (FTOA or FTOB).
The FTOA and FTOB output are "0" before the first compare-match.

Because OCRA and OCRB are 16-bit registers, a temporary register (TEMP) is used when they are written. See section 10.3, "CPU Interface" for details.

OCRA and OCRB are initialized to H'FFFF at a reset and in the standby modes.

10.2.3 Input Capture Register (ICR)—H'FF98, H'FFA8, H'FFB8

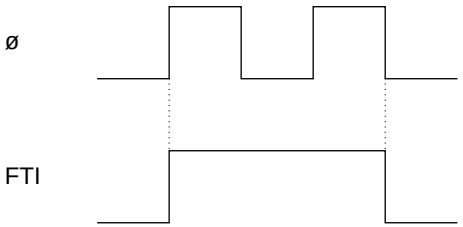
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

The ICR is a 16-bit read-only register.

When the rising or falling edge of the signal at the input capture input pin is detected, the current value of the FRC is copied to the ICR. At the same time, the input capture flag (ICF) in the timer control/status register (TCSR) is set to "1." The input capture edge is selected by the input edge select bit (IEDG) in the TCSR.

Because the ICR is a 16-bit register, a temporary register (TEMP) is used when the ICR is written or read. See section 10.3, "CPU Interface" for details.

To ensure input capture, the pulse width of the input capture signal should be at least 1.5 system clock periods (1.5·ø).



Minimum FTI Pulse Width

The ICR is initialized to H'0000 at a reset and in the standby modes.

Note: When input capture is detected, the FRC value is transferred to the ICR even if the input capture flag (ICF) is already set.

10.2.4 Timer Control Register (TCR)

Bit	7	6	5	4	3	2	1	0
	ICIE	OCIEB	OCIEA	OVIE	OEB	OEA	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The TCR is an 8-bit readable/writable register that selects the FRC clock source, enables the output compare signals, and enables interrupts.

The TCR is initialized to H'00 at a reset and in the standby modes.

Bit 7—Input Capture Interrupt Enable (ICIE): This bit selects whether to request an input capture interrupt (ICI) when the input capture flag (ICF) in the timer status/control register (TCSR) is set to “1.”

Bit 7 ICIE	Description	
0	The input capture interrupt request (ICI) is disabled.	(Initial value)
1	The input capture interrupt request (ICI) is enabled.	

Bit 6—Output Compare Interrupt Enable B (OCIEB): This bit selects whether to request output compare interrupt B (OCIB) when output compare flag B (OCFB) in the timer status/control register (TCSR) is set to “1.”

Bit 6

OCIEB	Description
0	Output compare interrupt request B (OCIB) is disabled. (Initial value)
1	Output compare interrupt request B (OCIB) is enabled.

Bit 5—Output Compare Interrupt Enable A (OCIEA): This bit selects whether to request output compare interrupt A (OCIA) when output compare flag A (OCFA) in the timer status/control register (TCSR) is set to "1."

Bit 5

OCIEA	Description
0	Output compare interrupt request A (OCIA) is disabled. (Initial value)
1	Output compare interrupt request A (OCIA) is enabled.

Bit 4—Timer overflow Interrupt Enable (OVIE): This bit selects whether to request a free-running timer overflow interrupt (FOVI) when the timer overflow flag (OVF) in the timer status/control register (TCSR) is set to "1."

Bit 4

OVIE	Description
0	The free-running timer overflow interrupt request (FOVI) is disabled. (Initial value)
1	The free-running timer overflow interrupt request (FOVI) is enabled.

Bit 3—Output Enable B (OEB): This bit selects whether to enable or disable output of the logic level selected by the OLVLB bit in the timer status/control register (TCSR) at the output compare B pin when the FRC and OCRB values match.

Bit 3

OEB	Description
0	Output compare B output is disabled. (Initial value)
1	Output compare B output is enabled.

Bit 2—Output Enable A (OEA): This bit selects whether to enable or disable output of the logic level selected by the OLVLA bit in the timer status/control register (TCSR) at the output compare A pin when the FRC and OCRA values match.

Bit 2 OEA	Description	
0	Output compare A output is disabled.	(Initial value)
1	Output compare A output is enabled.	

Bits 1 and 0—Clock Select (CKS1 and CKS0): These bits select external clock input or one of three internal clock sources for the FRC. External clock pulses are counted on the rising edge.

Bit 1 CKS1	Bit 0 CKS0	Description	
0	0	Internal clock source (ø/4)	(Initial value)
0	1	Internal clock source (ø/8)	
1	0	Internal clock source (ø/32)	
1	1	External clock source (counted on the rising edge)*	

* Output enable bit (bit 3) must be cleared to “0.”

10.2.5 Timer Control/Status Register (TCSR)

Bit	7	6	5	4	3	2	1	0
	ICF	OCFB	OCFA	OVF	OLVLB	OLVLA	IEDG	CCLRA
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W

The TCSR is an 8-bit readable and partially writable* register that selects the input capture edge and output compare levels, and specifies whether to clear the counter on compare-match A. It also contains four status flags.

The TCSR is initialized to H'00 at a reset and in the standby modes.

* Software can write a “0” in bits 7 to 4 to clear the flags, but cannot write a “1” in these bits.

Bit 7—Input Capture Flag (ICF): This status flag is set to “1” to indicate an input capture event. It signifies that the FRC value has been copied to the ICR.

Bit 7

ICF	Description
0	This bit is cleared from 1 to 0 when: (Initial value) 1. The CPU reads the ICF bit, then writes a “0” in this bit. 2. The data transfer controller (DTC) serves an input capture interrupt.
1	This bit is set to 1 when an input capture signal causes the FRC value to be copied to the ICR.

Bit 6—Output Compare Flag B (OCFB): This status flag is set to “1” when the FRC value matches the OCRB value.

Bit 6

OCFB	Description
0	This bit is cleared from 1 to 0 when: (Initial value) 1. The CPU reads the OCFB bit, then writes a “0” in this bit. 2. The data transfer controller (DTC) serves output compare interrupt B.
1	This bit is set to 1 when FRC = OCRB.

Bit 5—Output Compare Flag A (OCFA): This status flag is set to “1” when the FRC value matches the OCRA value.

Bit 5

OCFA	Description
0	This bit is cleared from 1 to 0 when: (Initial value) 1. The CPU reads the OCFA bit, then writes a “0” in this bit. 2. The data transfer controller (DTC) serves output compare interrupt A.
1	This bit is set to 1 when FRC = OCRA.

Bit 4—Timer Overflow Flag (OVF): This status flag is set to “1” when the FRC overflows (changes from H'FFFF to H'0000).

Bit 4

OVF	Description
0	This bit is cleared from 1 to 0 when the CPU reads the OVF bit, then writes a “0” in this bit. (Initial value)
1	This bit is set to 1 when FRC changes from H'FFFF to H'0000.

Bit 3—Output Level B (OLVLB): This bit selects the logic level to be output at the FTOB pin when the FRC and OCRB values match.

Bit 3

OLVLB	Description	
0	A “0” logic level (Low) is output for compare-match B.	(Initial value)
1	A “1” logic level (High) is output for compare-match B.	

Bit 2—Output Level A (OLVLA): This bit selects the logic level to be output at the FTOA pin when the FRC and OCRA values match.

Bit 2

OLVLA	Description	
0	A “0” logic level (Low) is output for compare-match A.	(Initial value)
1	A “1” logic level (High) is output for compare-match A.	

Bit 1—Input Edge Select (IEDG): This bit selects whether to capture the count on the rising or falling edge of the input capture signal.

Bit 1

IEDG	Description	
0	The FRC value is copied to the ICR on the falling edge of the input capture signal.	(Initial value)
1	The FRC value is copied to the ICR on the rising edge of the input capture signal.	

Bit 0—Counter Clear A (CCLRA): This bit selects whether to clear the FRC at compare-match A (when the FRC and OCRA values match).

Bit 0

CCLRA	Description
0	The FRC is not cleared. (Initial value)
1	The FRC is cleared at compare-match A.

10.3 CPU Interface

The FRC, OCRA, OCRB, and ICR are 16-bit registers, but they are connected to an 8-bit data bus. When the CPU accesses these four registers, to ensure that both bytes are written or read simultaneously, the access is performed using an 8-bit temporary register (TEMP).

These registers are written and read as follows.

- Register Write
  When the CPU writes to the upper byte, the upper byte of write data is placed in TEMP. Next, when the CPU writes to the lower byte, this byte of data is combined with the byte in TEMP and all 16 bits are written in the register simultaneously.
- Register Read
  When the CPU reads the upper byte, the upper byte of data is sent to the CPU and the lower byte is placed in TEMP. When the CPU reads the lower byte, it receives the value in TEMP.

Programs that access these four registers should normally use word access. Equivalently, they may access first the upper byte, then the lower byte. Data will not be transferred correctly if the bytes are accessed in reverse order, or if only one byte is accessed.

Coding Examples : Write the contents of R0 into OCRA in FRT1

```
        MOV.W R0, @H'FF94
    : Read ICR of FRT2
        MOV.W, @H'FFA8, R0
```

The same considerations apply to access by the DTC.

Figure 10-2 shows the data flow when the FRC is accessed. The other registers are accessed in the same way, except that when OCRA or OCRB is read, the upper and lower bytes are both transferred directly to the CPU without using the temporary register.

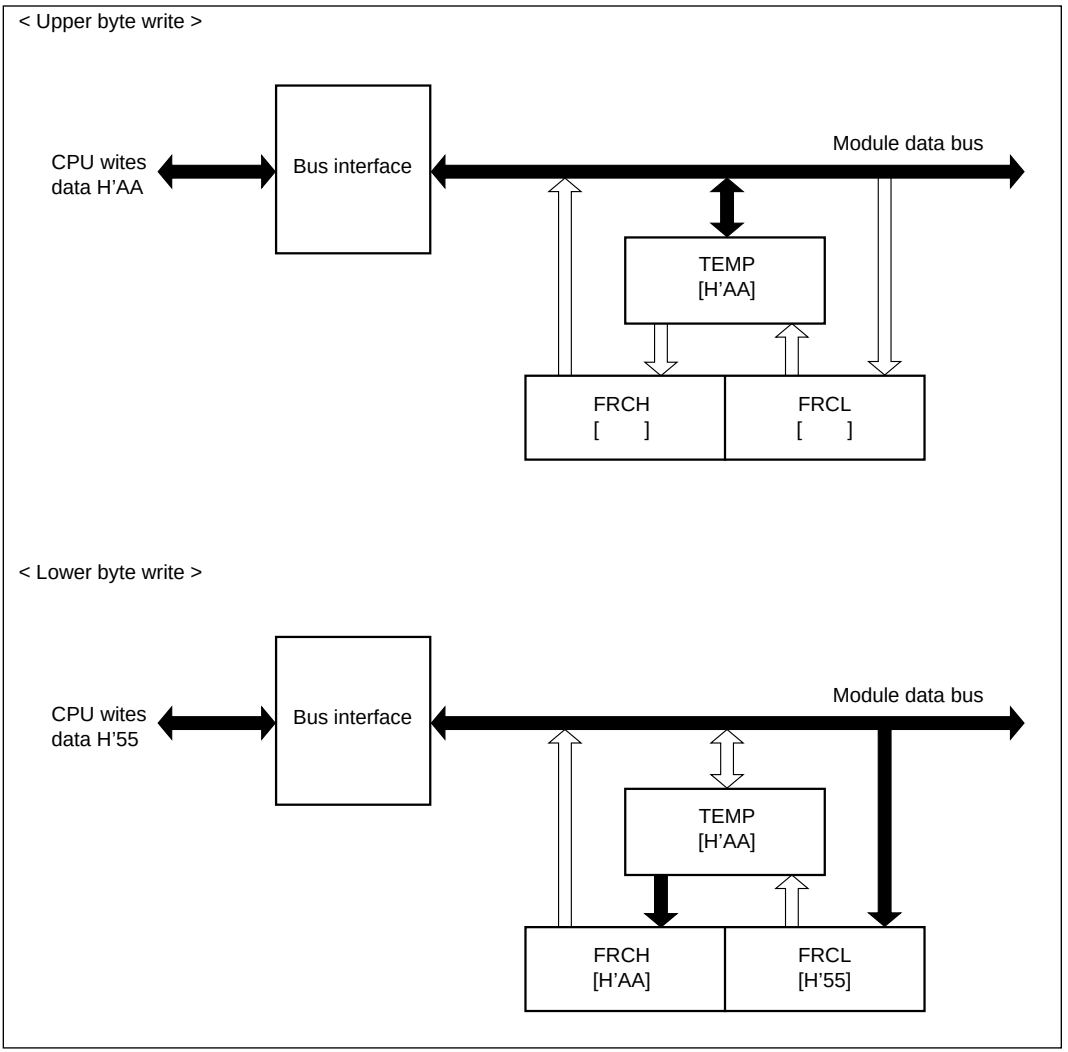


Figure 10-2 (a) Write Access to FRC (When CPU Writes H'AA55)

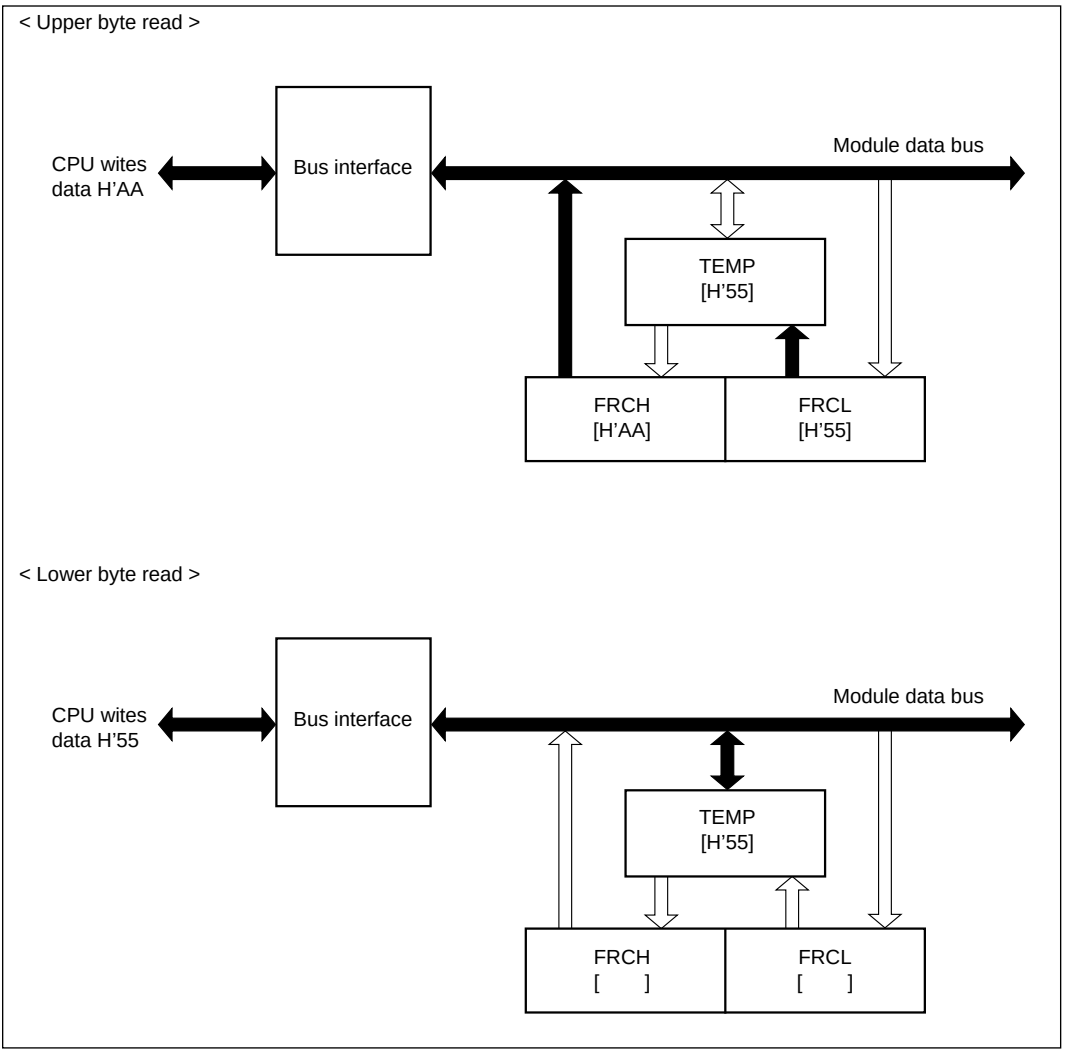


Figure 10-2 (b) Read Access to FRC (When FRC Contains H'AA55)

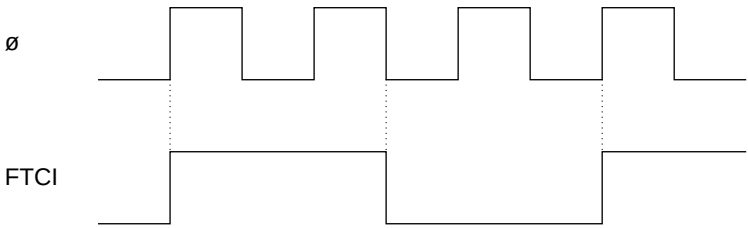
10.4 Operation

10.4.1 FRC Incrementation Timing

The FRC increments on a pulse generated once for each period of the selected (internal or external) clock source.

If external clock input is selected, the FRC increments on the rising edge of the clock signal. Figure 10-3 shows the increment timing.

The pulse width of the external clock signal must be at least 1.5·ø clock periods. The counter will not increment correctly if the pulse width is shorter than 1.5·ø clock periods.



Minimum FTCI Pulse Width

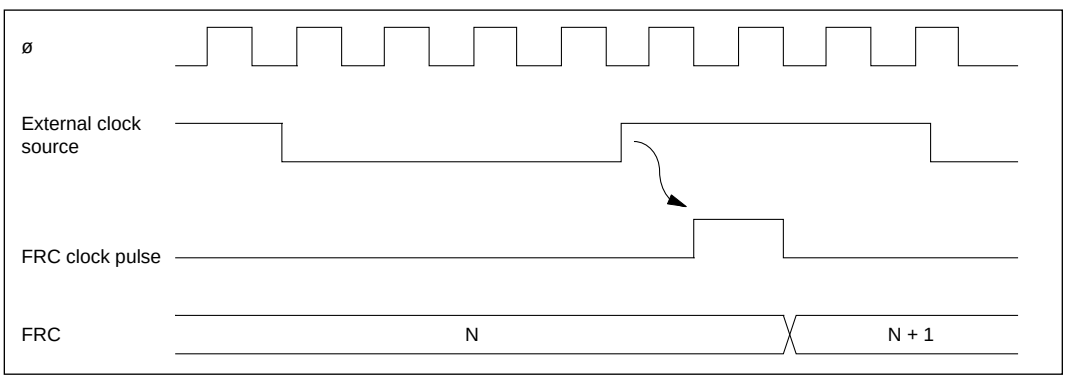


Figure 10-3 Increment Timing for External Clock Input

10.4.2 Output Compare Timing

Setting of Output Compare Flags A and B (OCFA and OCFB): The output compare flags are set to "1" by an internal compare-match signal generated when the FRC value matches the OCRA or OCRB value. This compare-match signal is generated at the last state in which the two values match, just before the FRC increments to a new value.

Accordingly, when the FRC and OCR values match, the compare-match signal is not generated until the next period of the clock source. Figure 10-4 shows the timing of the setting of the output compare flags.

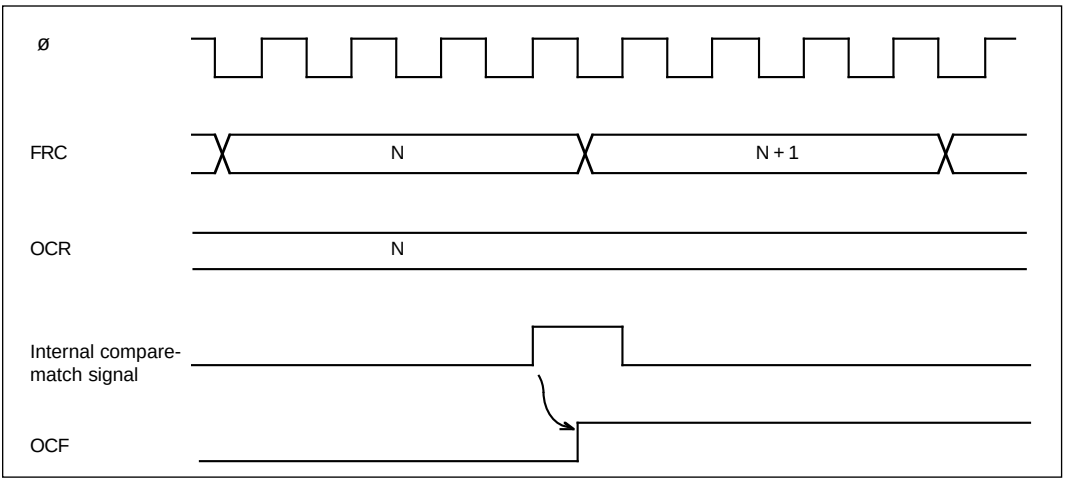


Figure 10-4 Setting of Output Compare Flags

Output Timing: When a compare-match occurs, the logic level selected by the output level bit (OLVLA or OLVLB) in the TCSR is output at the output compare pin (FTOA or FTOB). Figure 10-5 shows the timing of this operation for compare-match A.

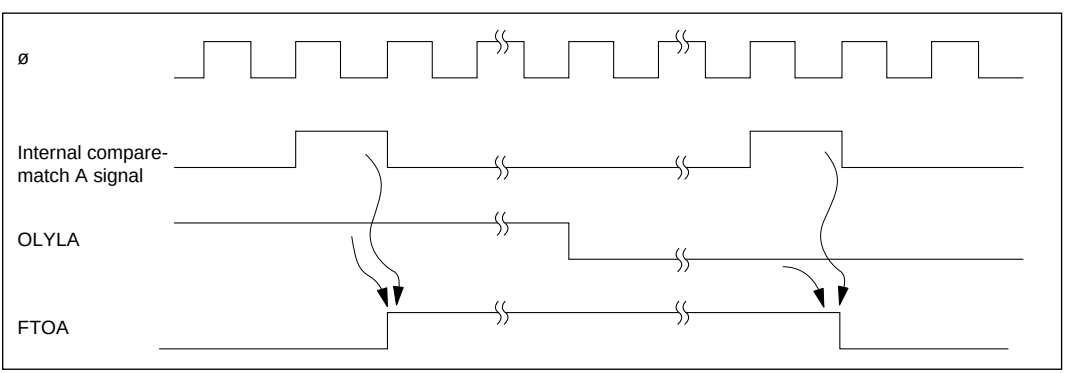


Figure 10-5 Timing of Output Compare A

FRC Clear Timing: If the CCLRA bit is set to "1," the FRC is cleared when compare-match A occurs. Figure 10-6 shows the timing of this operation.

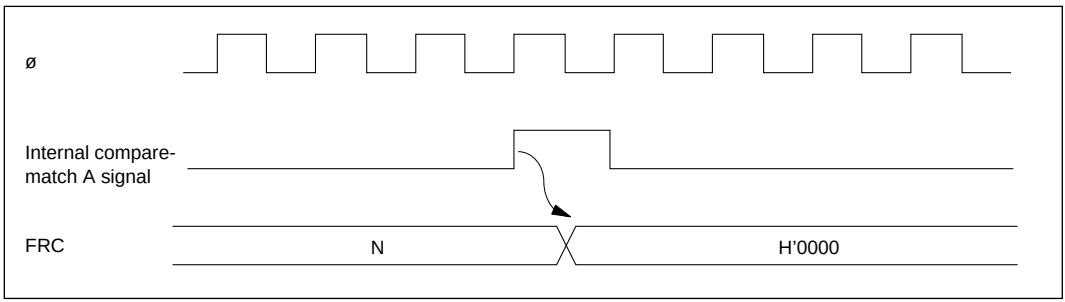


Figure 10-6 Clearing of FRC by Compare-Match A

10.4.3 Input Capture Timing

1. **Input Capture Timing:** An internal input capture signal is generated from the rising or falling edge of the input at the input capture pin (FTI), as selected by the IEDG bit in the TCSR. Figure 10-7 shows the usual input capture timing when the rising edge is selected (IEDG = "1").

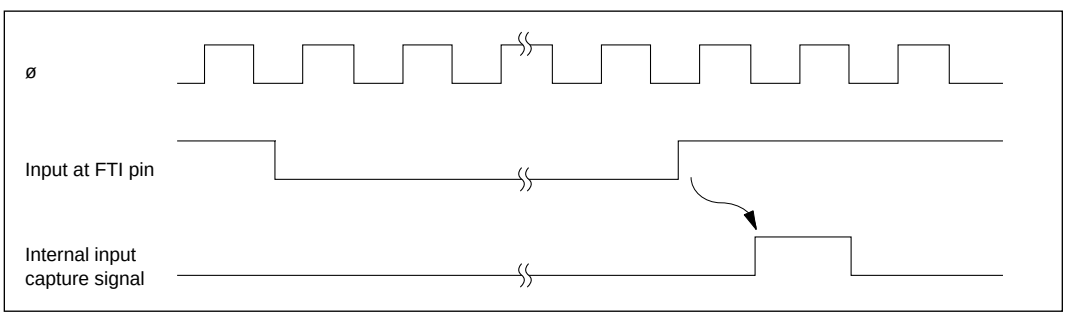


Figure 10-7 Input Capture Timing (Usual Case)

But if the upper byte of the ICR is being read when the input capture signal arrives, the internal input capture signal is delayed by one state. Figure 10-8 shows the timing for this case.

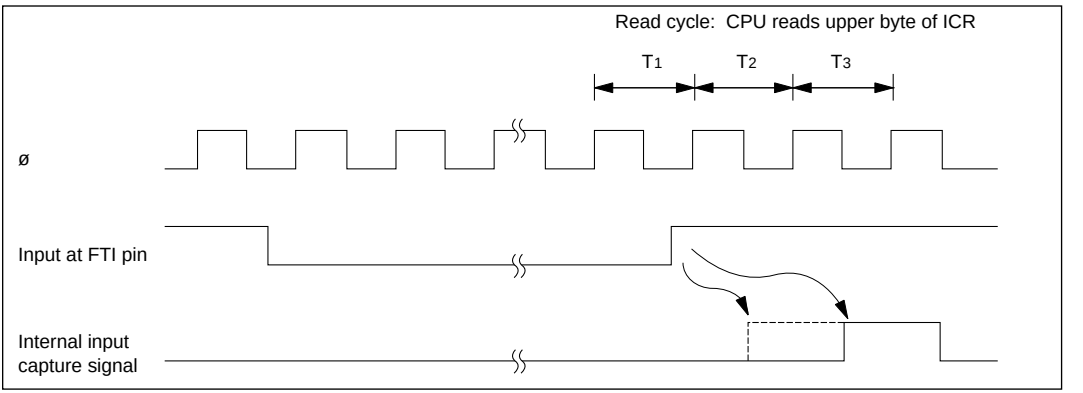


Figure 10-8 Input Capture Timing (1-State Delay)

Timing of Input Capture Flag (ICF) Setting: The input capture flag (ICF) is set to "1" by the internal input capture signal. Figure 10-9 shows the timing of this operation.

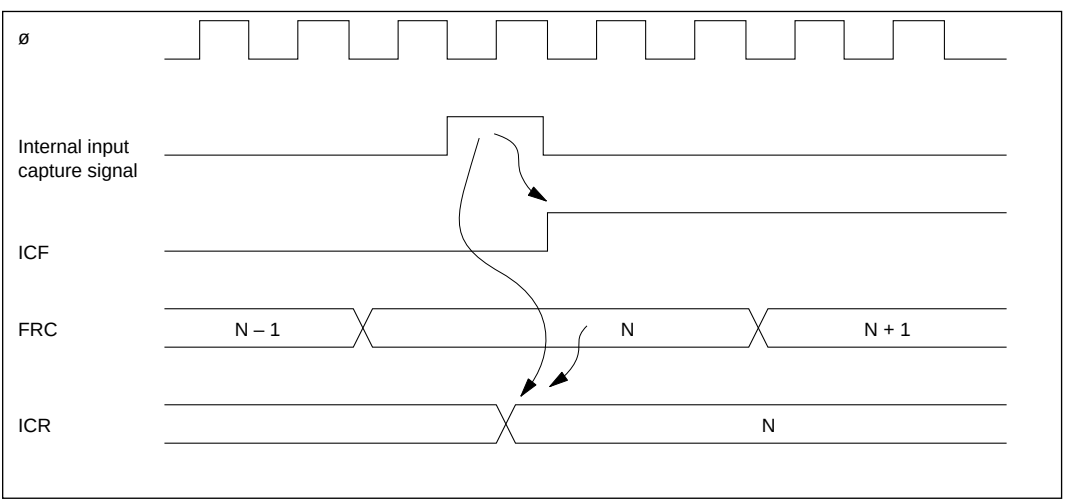


Figure 10-9 Setting of Input Capture Flag

10.4.4 Setting of FRC Overflow Flag (OVF)

The FRC overflow flag (OVF) is set to “1” when the FRC overflows (changes from H'FFFF to H'0000). Figure 10-10 shows the timing of this operation.

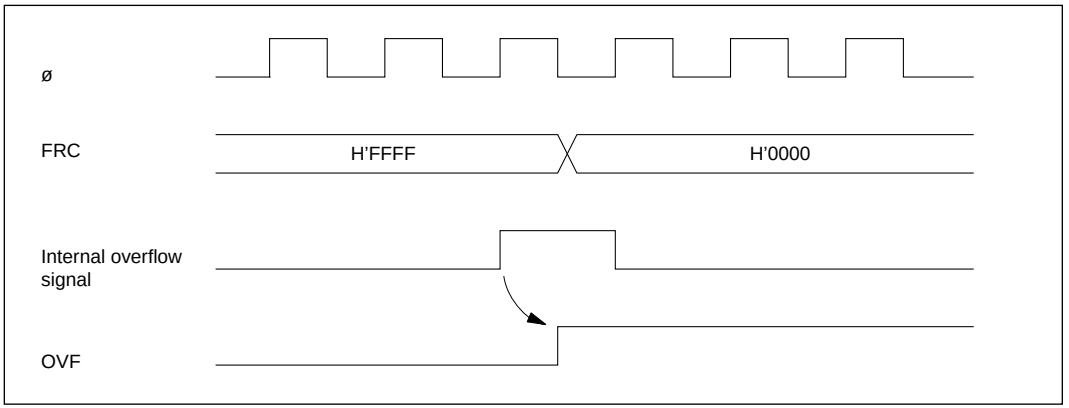


Figure 10-10 Setting of Overflow Flag (OVF)

10.5 CPU Interrupts and DTC Interrupts

Each free-running timer channel can request four types of interrupts: input capture (ICI), output compare A and B (OCIA and OCIB), and overflow (FOVI). Each interrupt is requested when the corresponding enable and flag bits are set. Independent signals are sent to the interrupt controller for each type of interrupt. Table 10-3 lists information about these interrupts.

Table 10-3 Free-Running Timer Interrupts

Interrupt	Description	DTC Service Available?	Priority
ICI	Requested when ICF is set	Yes	High
OCIA	Requested when OCFA is set	Yes	↑
OCIB	Requested when OCFB is set	Yes	
FOVI	Requested when OVF is set	No	Low

The ICI, OCIA, and OCIB interrupts can be directed to the data transfer controller (DTC) to have a data transfer performed in place of the usual interrupt-handling routine.

When the DTC serves one of these interrupts, it automatically clears the ICF, OCFA, or OCFB flag to “0.” See section 6, “Data Transfer Controller” for further information on the DTC.

10.6 Synchronization of Free-Running Timers 1 to 3

10.6.1 Synchronization after a Reset

The three free-running timer channels are synchronized at a reset and remained synchronized until:

- the clock source is changed;
- FRC contents are rewritten; or
- an FRC is cleared.

After a reset, each free-running counter operates on the ø/4 internal clock source.

10.6.2 Synchronization by Writing to FRCs

When synchronization among free-running timers 1 to 3 is lost, it can be restored by writing to the free-running counters.

Synchronization on Internal Clock Source: When an internal clock is selected, free-running timers 1 to 3 can be synchronized by writing data to their free-running counters as indicated in table 10-4.

Table 10-4 Synchronization by Writing to FRCs

Clock Source	Write Interval	Write Data	
ø/4	4n + 1 (states)	m	(FRC1)
ø/8	8n + 1 (states)	m + n	(FRC2)
ø/32	32n + 1 (states)	m + 2n	(FRC3)

m, n: Arbitrary integers

After writing these data, synchronization can be checked by reading the three free-running counters at the same interval as the write interval. If the read data have the same relative differences as the write data, the three free-running timers are synchronized.

Example a: ø/4 clock source, 12-state write interval (n = 3), on-chip memory

```
LA:   LDC.B #H'FF,BR        ; Initialize base register for short-format instruction (MOV:S)
      LDC.W #H'0700,SR      ; Raise interrupt mask level to 7
      MOV.W #m,R1           ; Data for free-running timer 1
      MOV.W #m+3,R2         ; Data for free-running timer 2 (m + n = m + 3)
      MOV.W #m+6,R3         ; Data for free-running timer 3 (m + 2n = m + 2 × 3)
      BSR   SET4            ; Call write routine
            :
      .ALIGN 2              ; Align write instructions (MOV:S) at even address
SET4: MOV:S.W R1,@H'92:8    ; Write to FRC 1 (address H'FF92)   9 states
      BRN SET4:8            ; 2-Byte dummy instruction          3 states
      MOV:S.W R2,@H'A2:8    ; Write to FRC 2 (address H'FFA2)        Total 12 states
      BRN SET4:8            ; 2-Byte dummy instruction
      MOV:S.W R3,@H'B2:8    ; Write to FRC 3 (address H'FFB2)
      RTS
```

Example b: ø/8 clock source, 16-state write interval (n = 2), on-chip memory

```
LB:   LDC.B #H'FF,BR
      LDC.W #H'0700,SR
      MOV.W #m,R1
      MOV.W #m+2,R2
      MOV.W #m+4,R3
      BSR   SET8
            :
      .ALIGN 2
SET8: MOV:S.W R1,@H'92:8          ; 9 States
      BRN SET8:8                  ; 3 States      Total 16 states
      XCH R1,R1                   ; 4 States
      MOV:S.W R2,@H'A2:8
      BRN SET8:8
      XCH R2,R2
      MOV:S.W R3,@H'B2:8
      RTS
```

Example c: ø/32 clock source, 32-state write interval (n = 1), on-chip memory

```
LC:     LDC.B #H'FF,BR
        LDC.W #H'0700,SR
        MOV.W #m,R1
        MOV.W #m+1,R2
        MOV.W #m+2,R3
        BSR   SET32
              :
        .ALIGN 2                        ; Align on even address
SET32:  MOV:S.W R1,@H'92:8              ; 2 Bytes, 9 states
        BSR WAIT:8                      ; 2 Bytes, 9 states
        MOV:S.W R2,@H'A2:8
        BSR WAIT:8                                          Total 32 states
        MOV:S.W R3,@H'B2:8
        RTS

        .ALIGN 2                        ; Align on even address
WAIT:   NOP                             ; 2 States
        XCH  R1,R1                      ; 4 States
        RTS                             ; 8 States
```

Note: The stack is assumed to be in on-chip RAM.

Example d: ø/4 clock source, 20-state write interval (n = 5), external memory

```
LD:     LDC.B  #H'FF,BR
        LDC.W  #H'0700,SR               ; Set interrupt mask level to 7
        CLR.B  @H'F8:8                  ; Disable wait states
        MOV.W  #m,R1
        MOV.W  #m+5,R2
        MOV.W  #m+10,R3
        MOV:S.W R1,@H'92:8              ; 13 States
        BRN    LD:8                     ; 2 Bytes, 7 states      Total 20 states
        MOV:S.W R2,@H'A2:8
        BRN    LD:8
        MOV:S.W R3,@H'B2:8
```

Example e: ø/8 clock source, 24-state write interval (n = 3), external memory

```
LE:  LDC.B #H'FF,BR
     LDC.W #H'0700,SR
     CLR.B @H'F8"8
     MOV.W #m,R1
     MOV.W #m+3,R2
     MOV.W #m+6,R3
     MOV:S.W R1,@H'92:8      ; 13 States
     BRN   LE:8              ; 2 Bytes,        7 states
     NOP                     ; 1 Byte,         4 states
     MOV:S.W R2,@H'A2:8
     BRN   LE:8
     NOP
     MOV:S.W R3,@H'B2:8
```

Total 24 states

Example f: ø/32 clock source, 32-state write interval (n = 1), external memory

```
LF:  LDC.B #H'FF,BR
     LDC.W #H'0700,SR
     CLR.B @H'F8:8
     MOV.W #m,R1
     MOV.W #m+1,R2
     MOV.W #m+2,R3
     MOV:S.W R1,@H'92:8      ; External memory, so 13 states
     XCH   R0,R0             ;                     8 states
     BRN   LF:8              ; 2 Bytes,            7 states
     NOP                     ;                     4 states
     MOV:S.W R2,@H'A2:8
     XCH   R0,R0
     BRN   LF:8
     NOP
     MOV:S.W R3,@H'B2:8
```

Total 32 states

Synchronization on External Clock Source: When the external clock source is selected, the free-running timers can be synchronized by halting their external clock inputs, then writing identical values in their free-running counters.

10.7 Sample Application

In the example below, one free-running timer channel is used to generate two square-wave outputs with a 50% duty factor and arbitrary phase relationship. The programming is as follows:

1. The CCLRA bit in the TCSR is set to "1."
2. Each time a compare-match interrupt occurs, software inverts the corresponding output level bit in the TCSR.

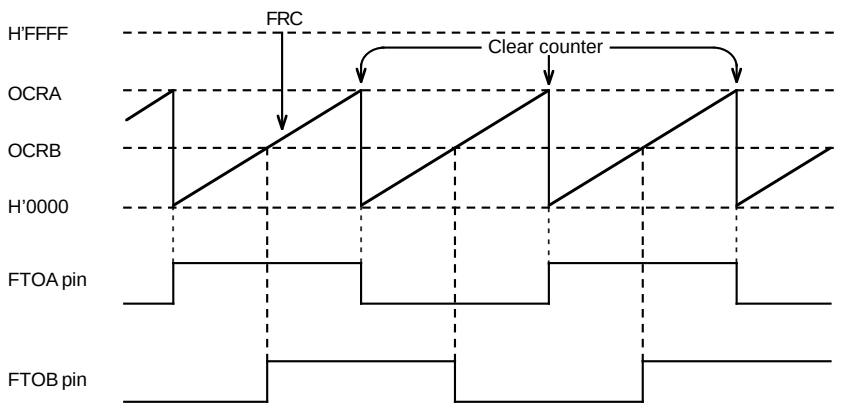


Figure 10-11 Square-Wave Output (Example)

10.8 Application Notes

Application programmers should note that the following types of contention can occur in the free-running timers.

Contention between FRC Write and Clear: If an internal counter clear signal is generated during the T_3 state of a write cycle to the lower byte of a free-running counter, the clear signal takes priority and the write is not performed.

Figure 10-12 shows this type of contention.

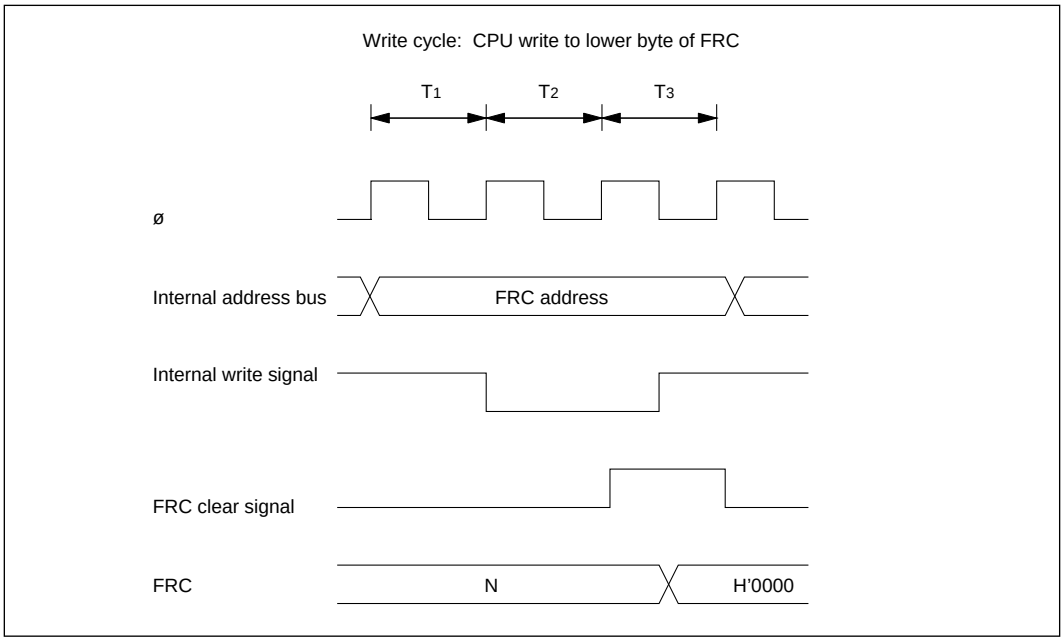


Figure 10-12 FRC Write-Clear Contention

Contention between FRC Write and Increment: If an FRC increment pulse is generated during the T3 state of a write cycle to the lower byte of a free-running counter, the write takes priority and the FRC is not incremented.

Figure 10-13 shows this type of contention.

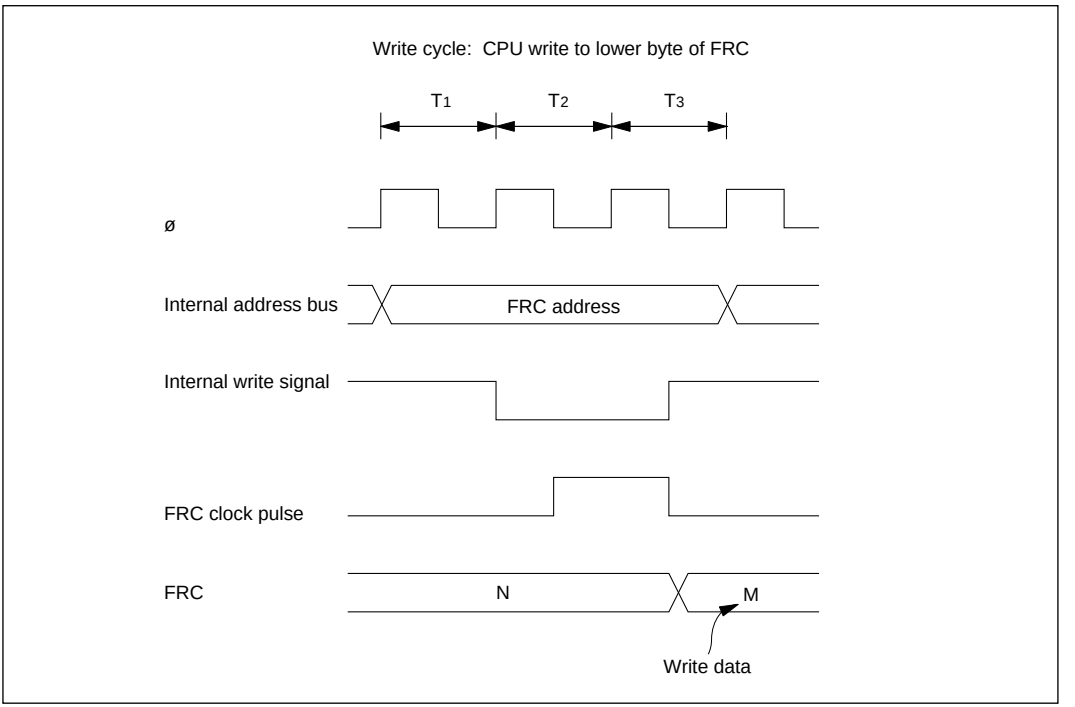


Figure 10-13 FRC Write-Increment Contention

Contention between OCR Write and Compare-Match: If a compare-match occurs during the T3 state of a write cycle to the lower byte of OCRA or OCRB, the write takes precedence and the compare-match signal is inhibited.

Figure 10-14 shows this type of contention.

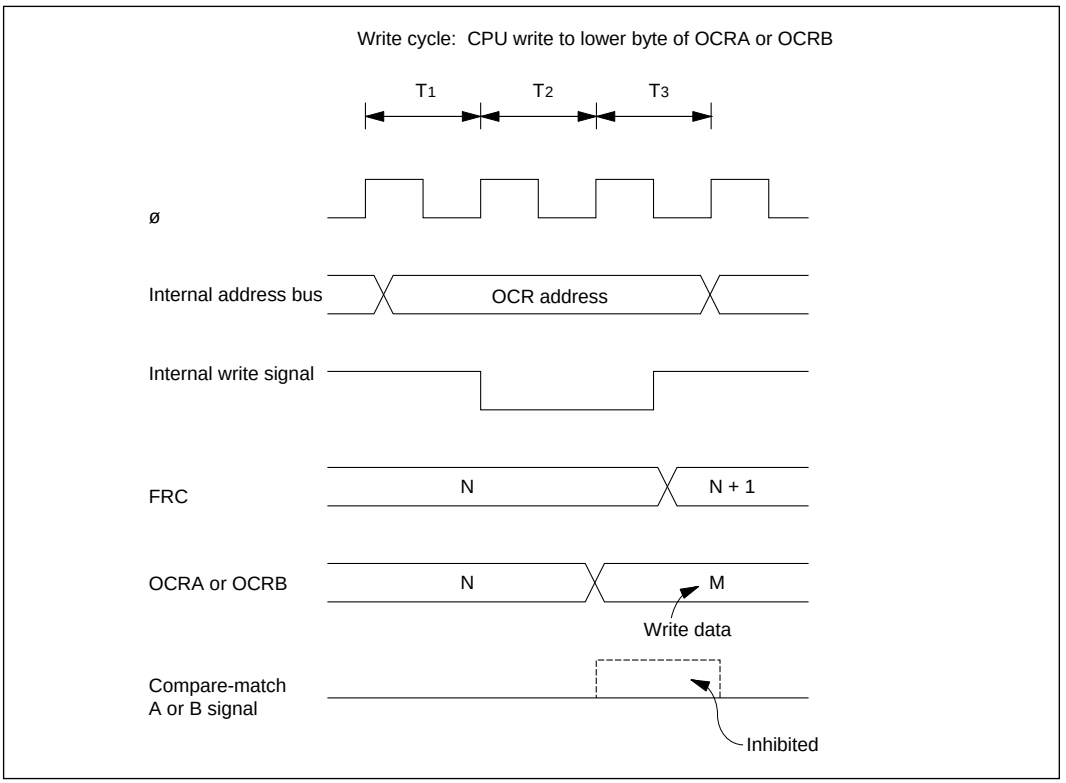


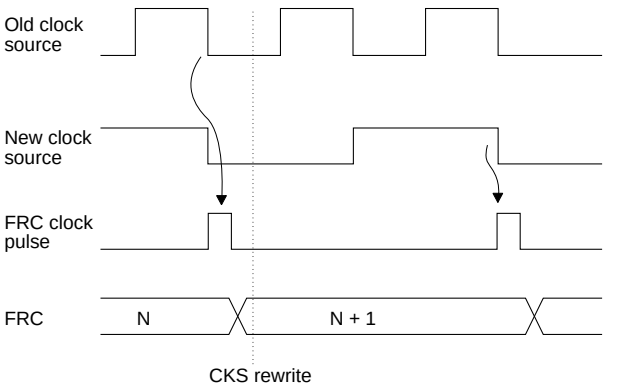
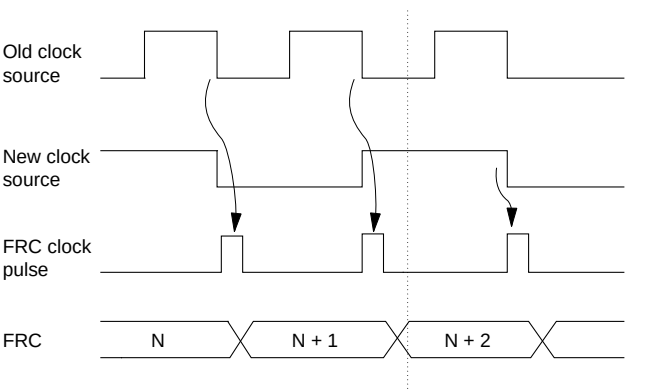
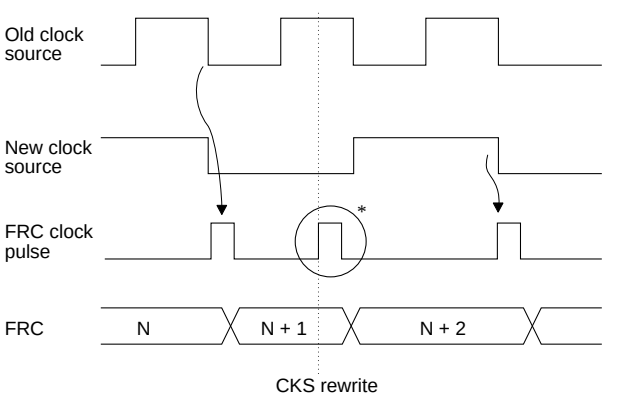
Figure 10-14 Contention between OCR Write and Compare-Match

Incrementation Caused by Changing of Internal Clock Source: When an internal clock source is changed, the changeover may cause the FRC to increment. This depends on the time at which the clock select bits (CKS1 and CKS0) are rewritten, as shown in table 10-5.

The pulse that increments the FRC is generated at the falling edge of the internal clock source. If clock sources are changed when the old source is High and the new source is Low, as in case No. 3 in table 10-5, the changeover generates a falling edge that triggers the FRC increment pulse.

Switching between an internal and external clock source can also cause the FRC to increment.

Table 10-5 Effect of Changing Internal Clock Sources

No.	Description	Timing Chart
1	Low → Low: CKS1 and CKS0 are rewritten while both clock sources are Low.	
2	Low → High: CKS1 and CKS0 are rewritten while old clock source is Low and new clock source is High.	
3	High → Low: CKS1 and CKS0 are rewritten while old clock source is High and new clock source is Low.	

∗ The switching of clock sources is regarded as a falling edge that increments the FRC.

Table 10-5 Effect of Changing Internal Clock Sources (cont)

No.	Description	Timing Chart
4	High → High: CKS1 and CKS0 are rewritten while both clock sources are High.